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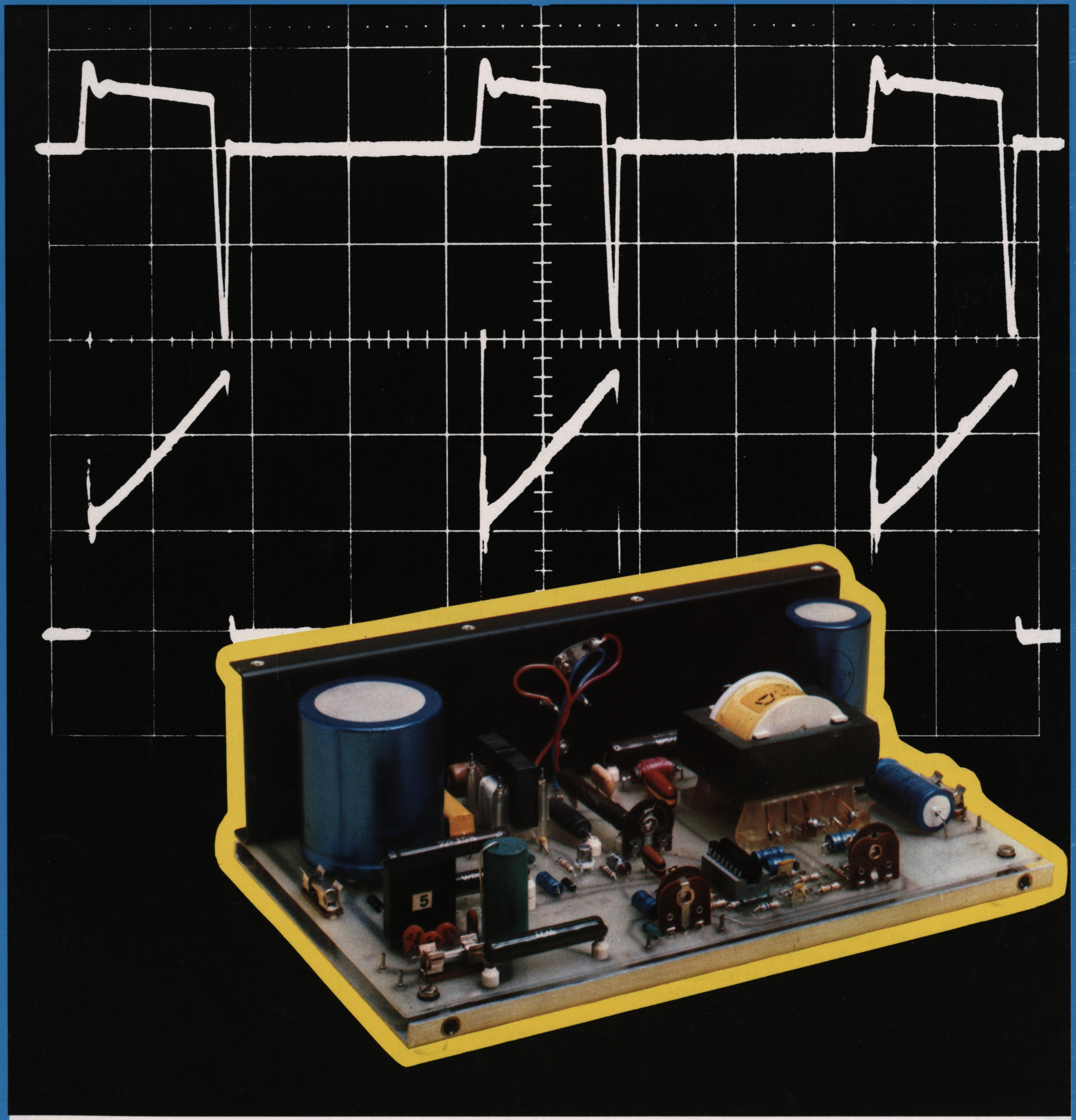

- Television switched-mode power supply using the TDA2640
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- An opto-isolated oscilloscope trigger circuit
- GZF1202 encoder and decoder for data error correction

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Cover picture:
Prototype television switched-mode power supply (version without mains isolation) together with output transistor base (upper) and collector (lower) current waveforms.

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Television switched-mode power supply using the TDA2640

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UDC 621.311.62: 621.397.132

This article describes a switched-mode power supply controlled by an integrated circuit, for colour television receivers. Circuits, layout, waveforms, and setting-up procedure are given.

INTRODUCTION

A colour tv receiver using transistor deflection circuits, such as the 20AX system, requires a power supply which provides a stabilised d.c. output (typically about 160V) with low ripple, from mains input voltages within the range from 180 to 265V r.m.s. The power supply must be inherently safe under overload conditions.

An established and satisfactory solution uses a thyristor operating as a phase-controlled rectifier to achieve stabilisation, and a resistance-capacitance filter to provide the necessary low ripple level. Fuses are normally used for overload protection. Such an arrangement provides acceptable performance at relatively low cost, but suffers from several fundamental limitations.

An alternative power supply concept using high-frequency switched-mode techniques offers the possibility of improved performance and extended flexibility in a number of areas. The most significant advantages of the switched-mode power supply, when compared with existing techniques using phase-controlled thyristor rectifiers, may be summarised as follows.

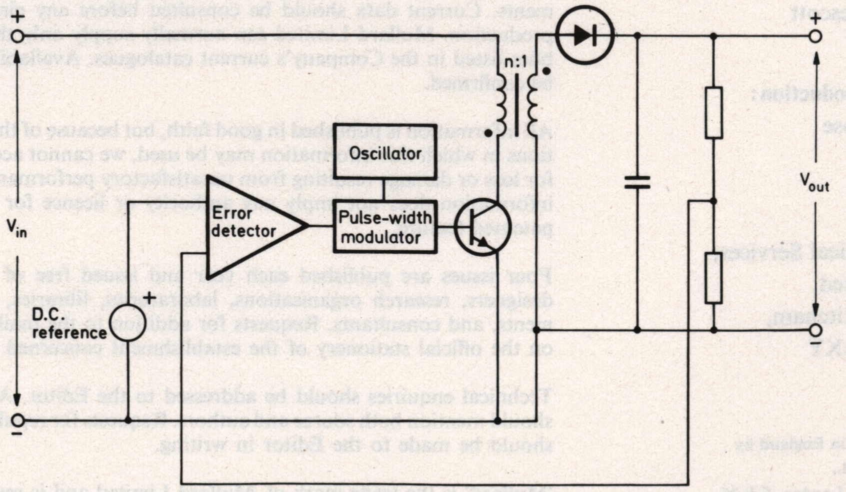

Fig.1 — Basic circuit of parallel switched-mode power supply

1) The improved efficiency of the SMPS leads to a considerable reduction in dissipated heat.
2) Comprehensive protection circuits are readily incorporated to deal with contingencies of overload and excessive output voltage, giving increased safety. Normal fusing merely provides a back-up.
3) Mains isolation of the receiver chassis can be achieved without the use of large 50Hz transformers.
4) Distortion of the mains supply waveform is reduced.
5) L.T. supplies can be derived in addition to the normal h.t. supply.

This article describes a switched-mode power supply for 110° colour tv receivers, using the TDA2640 integrated SMPS control circuit. The TDA2640 is intended to control power supplies of the single-ended switched-mode type: the circuit regulates the power supply output voltage by varying the duty cycle of the output switching transistor (pulse-width modulation).

The TDA2640 control IC provides:

1) duty cycle variation between 20 and 90%, with facilities to reduce the maximum duty cycle to less than 50%;
2) a slow-start circuit, to avoid excessive inrush currents at power supply switch-on;
3) protection against overvoltage, overcurrent, low supply voltage, and output control loop faults;
4) optional synchronisation of the SMPS to an external frequency source;
5) a shut-down circuit with a counting facility for sensing a persistent fault;
6) an inhibiting circuit for remote control.

Two versions of the SMPS, employing the same basic circuit, are described. One version is suitable for receivers where a live chassis is acceptable and where the lowest cost is required. An alternative version provides mains isolation of the receiver chassis in accordance with the requirements of national and international safety specifications such as BS 415 and IEC Recommendation 65.

PRINCIPLES OF OPERATION

The need to minimise cost, whilst providing performance compatible with operation as a television power supply, implies the use of a simple form of single-ended d.c.-to-d.c. converter, such as the flyback or ringing-choke system. The circuit adopted is a flyback converter operating at a fixed frequency: the duty cycle is varied in order to control the output.

Operation of the system is best described with reference to the simplified circuit diagram, Fig.1. This shows the basic arrangement of a parallel switched-mode system, which is the basis of the present design. The principal components are an inductor (which may be a single winding or, as shown, may carry one or more secondary windings), a power switching transistor, an output rectifier and filter capacitor, and a control system. The control system is represented by the potentiometer feedback network, a d.c. reference source, and the error detector, oscillator, and pulse-width modulator.

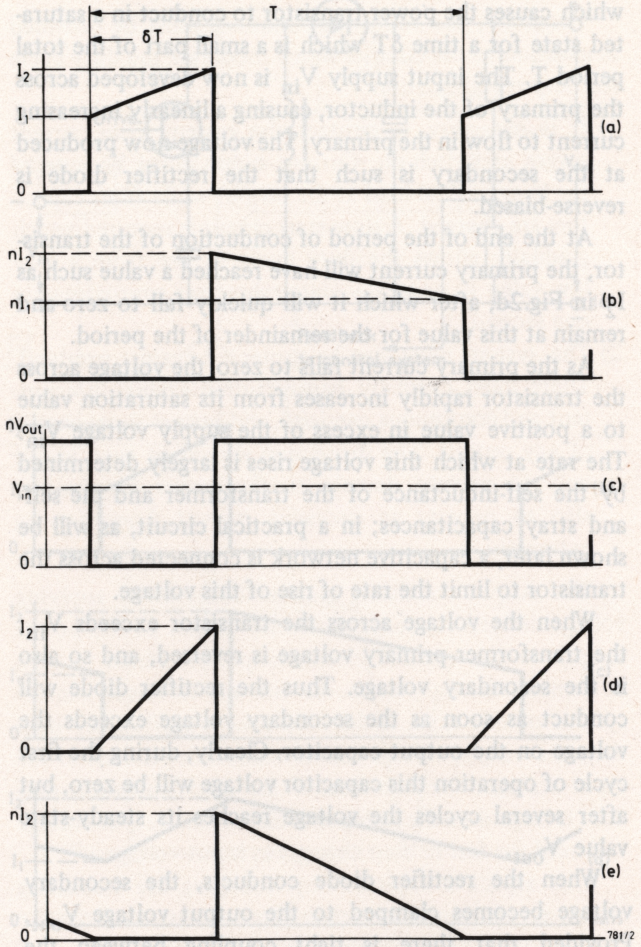

Fig.2 — Theoretical waveforms of parallel switched-mode power supply; (a) primary current; (b) rectifier current; (c) transistor V_{CE}, (d) primary current with critical value of inductances; (e) rectifier current with critical value of inductances

In practice, the d.c. input (V_{in}) is derived from rectification and partial smoothing of the a.c. mains to produce a supply voltage of the order of 300V.

Fig.2 shows the theoretical waveforms of current and voltage at various points in the circuit, under steady-state operating conditions.

Operation of the circuit is as follows. The oscillator free-runs, or is synchronised to an external reference, at a constant frequency typically within the range 16 to 20kHz; the period of oscillation is shown as T in Fig.2. Assume initially that the modulator produces an output which causes the power transistor to conduct in a saturated state for a time δT which is a small part of the total period T. The input supply V_{in} is now developed across the primary of the inductor, causing a linearly increasing current to flow in the primary. The voltage now produced at the secondary is such that the rectifier diode is reverse-biased.

At the end of the period of conduction of the transistor, the primary current will have reached a value such as I_2 in Fig.2d, after which it will quickly fall to zero and remain at this value for the remainder of the period.

As the primary current falls to zero, the voltage across the transistor rapidly increases from its saturation value to a positive value in excess of the supply voltage V_{in}. The rate at which this voltage rises is largely determined by the self-inductance of the transformer and the self- and stray capacitances; in a practical circuit, as will be shown later, a capacitive network is connected across the transistor to limit the rate of rise of this voltage.

When the voltage across the transistor exceeds V_{in}, the transformer primary voltage is reversed, and so also is the secondary voltage. Thus the rectifier diode will conduct as soon as the secondary voltage exceeds the voltage on the output capacitor. Clearly, during the first cycle of operation this capacitor voltage will be zero, but after several cycles the voltage reaches its steady-state value V_{out}.

When the rectifier diode conducts, the secondary voltage becomes clamped to the output voltage V_{out}. Provided that there is tight coupling between the transformer windings, the primary voltage cannot then exceed the product of the secondary voltage and the transformation ratio n. The primary voltage in a practical circuit contains a ringing component due to leakage reactance in the transformer; a damping network is connected across the primary to limit the amplitude of ringing voltages.

It can therefore be seen that there are two distinct operations in each cycle. First, the transistor conducts for a portion δT of the period, when energy is taken from the input supply and stored in the inductor. Second, during the remainder of the period, the rectifier diode conducts and the energy stored in the inductor is transferred to the output: initially to charge the capacitor, and under steady-state conditions to drive the load.

The output voltage is dependent upon the input voltage and also upon the proportion of the period for which the transistor is conducting (that is, the duty cycle δ). To stabilise the output voltage it is the function of the control system continuously to arrange a value of δ appropriate to the input voltage and loading, so that any change in these parameters causes a change in the conduction time of the transistor, and hence in the output voltage, which opposes the effect of the original change.

THEORY AND DESIGN CRITERIA

From the preceding description of the method of operation, some fundamental relationships can readily be established to enable a design to be developed. The master oscillator in the control circuit operates at constant frequency and therefore defines the period T. Similarly the control system establishes a value of the duty cycle δ necessary to achieve stabilisation at any instant.

It is convenient to make certain simplifying assumptions in order to establish the operating theory. Assume that the transistor operates as a perfect switch, and that the effect of storage time is included as part of the conduction period. The saturation and switching losses of the transistor are included with all the losses and represented by two loss resistances, one connected across the input and the other across the output. (Note that the power dissipated in the output losses is supplied through the transformer.)

During the first part of the cycle, with the transistor conducting, the current in the primary winding (Fig.2d) rises to a value I_2 given by:

$$I_2 = \frac{V_{in}\,\delta T}{L}.$$

This implies that at the end of the conduction time δT, the energy stored is:

$$W = \tfrac{1}{2} L I_2^{\,2} = \frac{V_{in}^{\;2}\,\delta^2\,T^2}{2L},$$

where L is the self-inductance of the transformer primary. This is the maximum stored energy per cycle, and hence the available power is given by:

$$P_o = Wf,$$

where f is the operating frequency. Since f = 1/T:

$$P_o = \frac{V_{in}^{\;2}\,\delta^2 T}{2L}. \qquad \ldots (1)$$

The quantity P_o represents the sum of the useful output power and those losses that are supplied through the transformer.

A second important relationship is established by consideration of the current waveform under steady-state conditions; clearly the positive increment of current during the conduction time δT must be exactly matched by a corresponding decrease during the remainder of the period. Thus:

$$\frac{V_{in}\,\delta T}{L} = \frac{nV_{out}\,(T - \delta T)}{L},$$

where n is the transformation ratio, and so:

$$V_{out} = \frac{V_{in}}{n}\,\frac{\delta}{(1-\delta)}. \qquad \ldots (2)$$

From Eq.2 it can be seen that, for a given transformation ratio, the output voltage depends on the input voltage and the duty cycle.

It is also apparent from Eqs.1 and 2 that for given values of input voltage, inductance, and frequency, only one value of P_o will completely dissipate all the available energy stored in the inductor. For this reason it is normally necessary to allow the frequency to vary when operation in this mode is used.

In the present case, with fixed-frequency operation, circuit values are arranged so that the stored energy at the end of each cycle is zero only with minimum load and maximum supply voltage (that is, with the highest possible value of the mains voltage). Under all other conditions of load and input, the fixed period T is shorter than the time required to extract all stored energy from the inductor, and so at the end of the cycle there will be stored energy remaining in the inductor. It follows that at the start of the next cycle, that is when the transistor starts to conduct, the initial current will not be zero as in Fig.2d, but will have a positive value such as I_1 (Fig.2a). The value of I_1 is related to the quantity of stored energy remaining in the inductor.

For any given combination of input voltage and output power, it can be seen that there is a choice of operating modes defined by the ratio of I_2 to I_1 and determined by the operating frequency and self-inductance of the transformer.

A limit case occurs when the stored energy is just sufficient to provide the output power and losses. In this case the primary current waveform is the sawtooth shown in Fig.2d. Another (theoretical) limit case is characterised by a rectangular current waveform, which implies an infinite value for the transformer self-inductance.

The general current waveform for the mode of operation used in this power supply is trapezoidal, as shown in Fig.2a, and the ratio I_2/I_1 is approximately 2 under normal operating conditions.

It is worth comparing the relative merits of operation with sawtooth and trapezoidal current waveforms. Assuming the same input and output requirements, sawtooth operation implies variable-frequency operation, and requires a higher value of peak current I_2. Trapezoidal operation allows the switching frequency to be fixed, and the peak current and ripple current are lower. However, a larger inductor is required because the energy stored is greater, and furthermore the higher turn-off current usually causes increased losses in the rectifier.

The required value of primary inductance is derived from Eq.1 where the output power is given its minimum value (that is, operation of the tv receiver at zero beam current, etc.) and the input voltage is given its maximum value. The minimum value of inductance then required is given by:

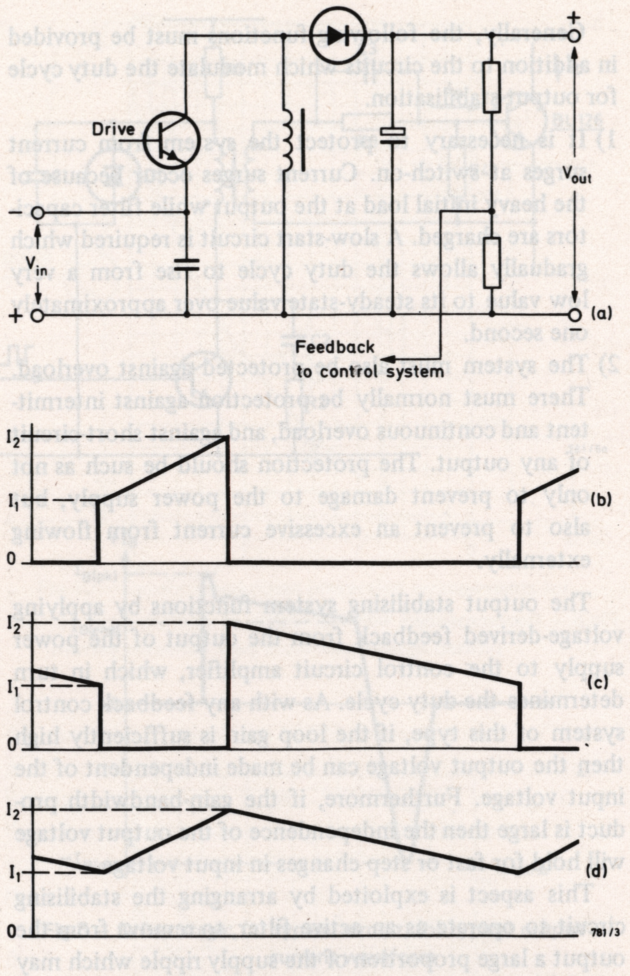

Fig.3 – Choke-coupled switched-mode power supply: (a) basic circuit; (b) transistor current waveform; (c) rectifier current waveform; (d) choke current waveform

$$L_{min} = \frac{V_{in(max)}^2\,\delta^2}{2P_{o(min)}\,f}.$$

The corresponding value for δ is derived from Eq.2 using the maximum value for V_{in}:

$$\delta = \frac{nV_{out}}{V_{in} + nV_{out}}.$$

The transformer turns ratio n may have a value of unity, as in the non-isolated version of the power supply. In this case a single transformer winding suffices for both the input and the output circuits. The basic circuit of this arrangement is shown in Fig.3a, and the corresponding theoretical waveforms in Figs.3b to 3d.

Control system

The control system consists of the small-signal circuits which regulate the conduction time of the power transistor, via a driver stage, according to the operating conditions.

Generally, the following functions must be provided in addition to the circuits which modulate the duty cycle for output stabilisation.

1) It is necessary to protect the system from current surges at switch-on. Current surges occur because of the heavy initial load at the output while filter capacitors are charged. A slow-start circuit is required which gradually allows the duty cycle to rise from a very low value to its steady-state value over approximately one second.
2) The system must also be protected against overload. There must normally be protection against intermittent and continuous overload, and against short-circuit of any output. The protection should be such as not only to prevent damage to the power supply, but also to prevent an excessive current from flowing externally.

The output stabilising system functions by applying voltage-derived feedback from the output of the power supply to the control circuit amplifier, which in turn determines the duty cycle. As with any feedback control system of this type, if the loop gain is sufficiently high then the output voltage can be made independent of the input voltage. Furthermore, if the gain-bandwidth product is large then the independence of the output voltage will hold for fast or step changes in input voltage.

This aspect is exploited by arranging the stabilising circuit to operate as an active filter, to remove from the output a large proportion of the supply ripple which may exist on the input. For reasons described below, it is undesirable to make the loop gain of the control circuit as large as would be necessary to achieve the high ripple attenuation desired. A ripple compensation circuit can be provided to achieve similar results.

In order to provide an adequate margin of stability it is normally necessary with this type of power supply to effect a compromise between stabilisation performance and loop gain. Where necessary a forward-acting control loop can be used to enhance the stabilisation in a similar way to the ripple compensation circuit.

The characteristics of several elements of the circuit combine to determine the overall performance in terms of linearity, gain, and stability margin. The most significant of these characteristics are illustrated in Fig.4, and may be summarised as comprising the transfer characteristics of the following:

1) the control amplifier A;
2) the feedback network (factor $B = Z_2/(Z_1 + Z_2)$; the turns ratio of the transformer may be considered part of the feedback network);
3) the resonant circuit formed by the transformer inductance and the filter capacitance, with damping due to the load resistance;

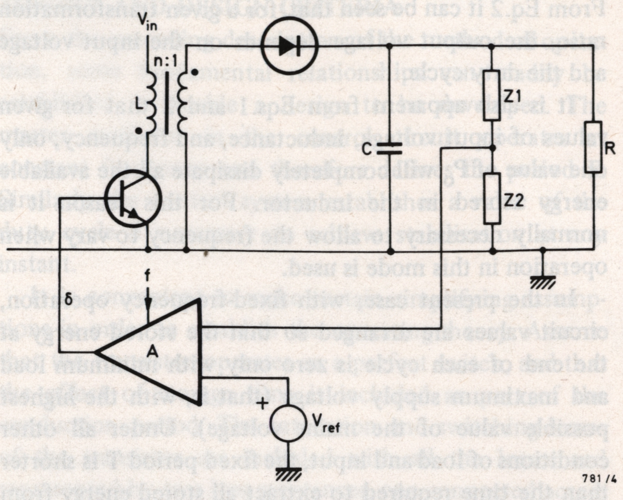

Fig.4 – Basic circuit of control system

4) the energy transfer process, defined by the relationship $V_{out} = V_{in}\ \delta/(1 - \delta)$;
5) the effect of the finite sampling rate determined by the switching frequency f.

For the type of power supply being considered, it is the LC resonance, item (3) above, which presents the major difficulty to the use of high loop gain. The resonance arises at a relatively low frequency, typically below 1kHz, and with high values of load resistance the damping will be light and large phase shifts will occur at frequencies approaching resonance. Thus with large amounts of gain, instability can arise. The result may be oscillation of the power supply at a frequency near this resonance.

To obtain a satisfactory solution, a compromise is required which provides acceptable stabilisation performance, adequate margin of stability, and satisfactory transient response. In the present case, these objectives have been achieved by using only moderate loop gain, and by appropriate choice of the feedback network.

The latter is arranged in two parts. The first part consists of the transformation ratio between the output voltage which requires to be regulated and the transformer winding providing the feedback voltage. This ratio is 5:1. The waveform delivered by the transformer winding is rectified, filtered, and loaded to provide acceptable tracking of the output supply, and then fed through a frequency-dependent divider network to the control amplifier.

Driver stage

The power transistor used in the output stage is the BU126. This is a high-voltage silicon n-p-n transistor in TO-3 encapsulation, specifically intended for use in switched-mode power supplies for colour television receivers.

As is usual with high-voltage power transistors, to ensure satisfactory operation as a saturated switching transistor, the driving circuit must provide base current in both forward and reverse directions. To minimise dissipation in the BU126, the base current waveform must produce an adequately small value of saturation voltage across the device during its conduction period, but must also allow fast turn-on and turn-off throughout the range of transistor spreads.

The driver stage must deliver the correct drive waveform within acceptable limits, over the specified range of mains supply voltages. Further important features of the driver stage are:

1) the ability to hold the power transistor cut off for long periods, for example if the protection circuits in the control system so require;
2) adequate current gain, to provide the correct interface between the power transistor and the control circuits;
3) correct reproduction of the drive current duty cycle determined by the control circuit: this necessitates a low value of driver stage storage delay.

A convenient driver stage arrangement which fulfils the above requirements makes use of a medium-voltage transistor, operating from the input supply via a high resistance, and transformer-coupled to the power transistor. The driver transistor operates non-simultaneously with respect to the output transistor. In this way, no additional low-voltage supply rails are required; further, by appropriate choice of the transistor V_{CE} and transformer turns ratio, the dissipation in the supply dropping resistance is acceptable. When the protection circuits are operating (for example under overload conditions), the driver transistor may remain in continuous saturation with the full supply voltage developed across the dropping resistor.

A typical circuit for this driver stage is shown in Fig.5 together with the BU126 base current waveform. The operation of the stage may be summarised as follows.

Forward base current is delivered to the BU126 by virtue of the stored energy in the transformer when the driver stage is cut off. During this period the value of base current cannot remain constant, but droops at a rate dependent upon the transformer inductance until it reaches the final value, $I_{B(end)}$. It should be noted that during this time the collector current of the BU126 is changing in the opposite direction as shown in Fig.2a; that is, increasing towards its final value $I_{C(end)}$. Thus the important values are $I_{C(end)}$, $I_{B(end)}$, and the base current droop ΔI_B, where:

$$\Delta I_B = I_{B(pk)} - I_{B(end)}.$$

If the general shape of the collector and base current waveforms is specified, then it is possible to specify an optimum value for $I_{B(end)}$ corresponding to a value of $I_{C(end)}$ over a certain range. This optimum value takes account of spreads in transistor characteristics and provides a satisfactory compromise between saturation and switching losses. For the BU126, Fig.6 gives the nominal value of the recommended base current $I_{B(end)}$ plotted against maximum peak collector current. (Maximum peak collector current occurs at maximum load and minimum input voltage.) Similarly, Fig.7 gives the total device dissipation P_{tot} versus maximum peak collector current. These values apply provided that the shape of the collector current waveform is such that the value of I_2/I_1 (as defined in Fig.2a) is greater than or equal to 2.

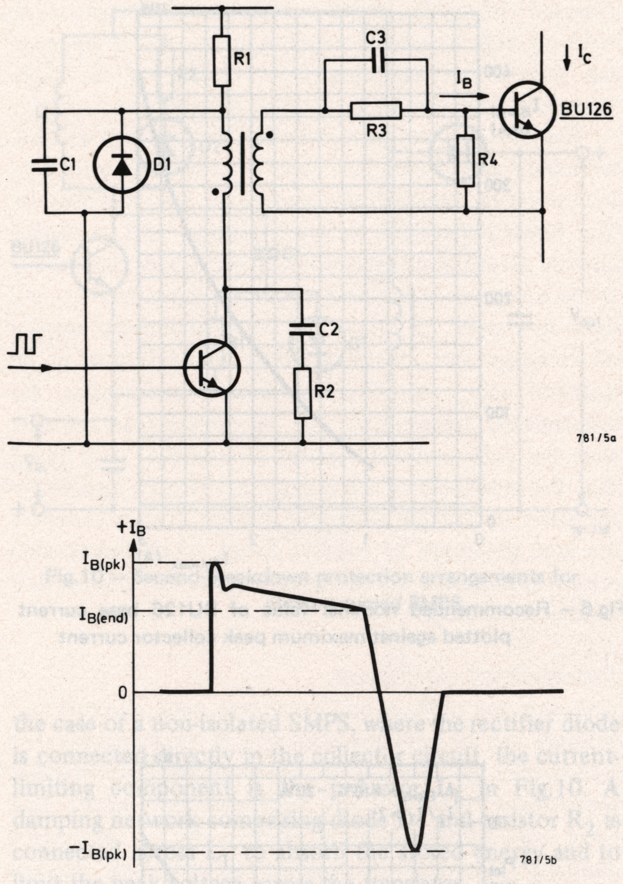

Fig.5 – Driver stage: (a) typical circuit; (b) typical output current waveform

The driver transformer inductance must be large enough to prevent excessive base current droop during the conduction period of the BU126. The required inductance of the secondary of the driver transformer is obtained from the relationship:

$$L_s = (E_B - V_{BE} - I_B R_3)\ \delta T/\Delta I_B,$$

where E_B is the forward drive voltage delivered from the secondary of the transformer, and ΔI_B is the acceptable

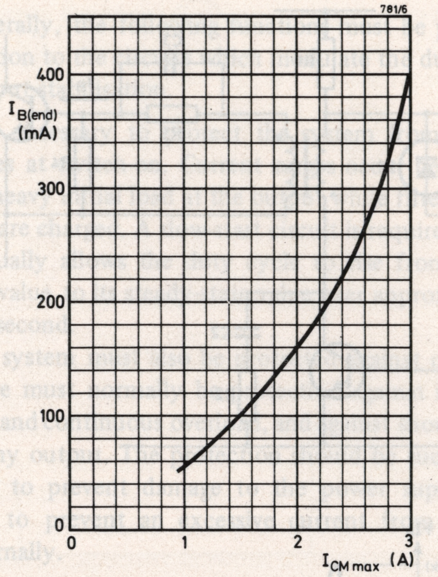

Fig.6 – Recommended nominal value of BU126 base current plotted against maximum peak collector current

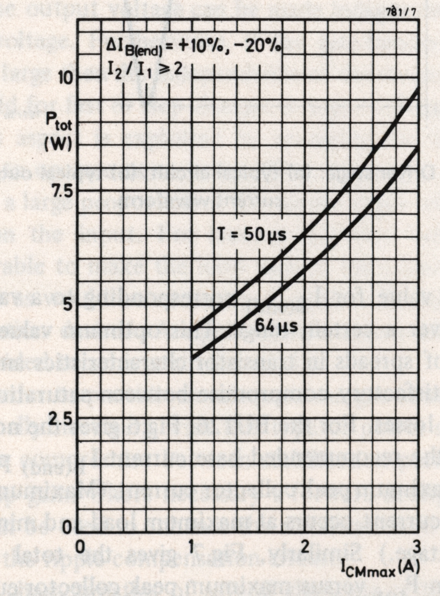

Fig.7 – Total BU126 dissipation plotted against maximum peak collector current

base current droop over the period δT. A typical value for L_s is 1mH.

To provide operating conditions within the safe operating area for the BU126, the reverse base drive waveform must be correct: it is of equal importance to the forward drive waveform. In the circuit of Fig.5, several components are included to provide optimum turn-off drive. Typical of these are the speed-up network (C_3 and R_3) in the base circuit of the BU126, and the low value of the decoupling capacitor C_1; the leakage inductance of the transformer is designed to provide the correct storage time for the BU126 as well as contributing to the turn-off energy.

Recommended turn-off waveforms for the BU126 are shown in Fig.8, and the safe operating area is shown in Fig.9. It is particularly important to ensure an adequate duration of reverse base current after the collector current of the BU126 starts to decrease, so that correct turn-off is provided even for limit devices; this duration is shown as t_2 in Fig.8.

Two further features of the driver circuit design must be explained. The first is the provision of a fast rise-time to the leading edge of the forward base current pulse. Fig.2a shows that the collector current of the BU126 at turn-on rises immediately to its initial value I_1; furthermore, in a practical circuit a spike will be added to this initial current, owing to collector circuit capacitances and storage effects in the output rectifiers. Because of this, and in order to reduce the turn-on dissipation, a fast-rising base current pulse is desirable: to achieve a fast rise of current, the network C_2R_2 (Fig.5a) is arranged to under-damp the transformer and provide a degree of overshoot.

The second point relates to the diode D_1 across the decoupling capacitor C_1. The purpose of this diode is to prevent a reversal of current in the transformer; without it, resonance in the transformer and C_1 could cause a spurious turn-on pulse to be applied to the BU126.

Output stage

The BU126 output transistor operates in a common-emitter configuration with a highly inductive collector load. To guarantee that the operating load line remains within the permitted safe operating area, and that second breakdown does not occur, it is necessary to include passive protection networks in the collector circuit.

Fig.10 shows the components of the output stage for a non-isolated choke-coupled system. A network comprising C_1, R_1, and D_1 is connected across the transistor. When the transistor cuts off, the inductive load tends to cause a rapid increase in the collector-emitter voltage: diode D_1 then conducts, switching the capacitor across the transistor. In conjunction with the self-inductance of the choke, this effectively reduces the rate of increase of V_{CE}. The component values are proportioned so that, 0·5μs after the collector current falls to 90% of its peak value, the value of V_{CE} does not exceed 500V. This value is shown in Fig.8 as $V_{CE}(t_1)$.

Because of the effects of the reverse recovery charge in the output rectifier, and to a lesser extent the self-capacitances of the collector circuit and the transformer, a large collector current flows in the BU126 at the instant of turn-on. To limit this peak current, an impedance is required in series with the transistor and h.t. rectifier. In the case of a non-isolated SMPS, where the rectifier diode is connected directly in the collector circuit, the current-limiting component is the inductor L_1 in Fig.10. A damping network comprising diode D_2 and resistor R_2 is connected across L_1 to absorb the stored energy and to limit the peak voltage across the transistor.

In the case of a mains-isolated SMPS, the rectifier diode is coupled to the collector circuit by the isolating output transformer; the leakage inductance of the transformer may then serve to provide the current-limiting impedance, taking the place of L_1. A damping network will then be required across the primary winding of the transformer.

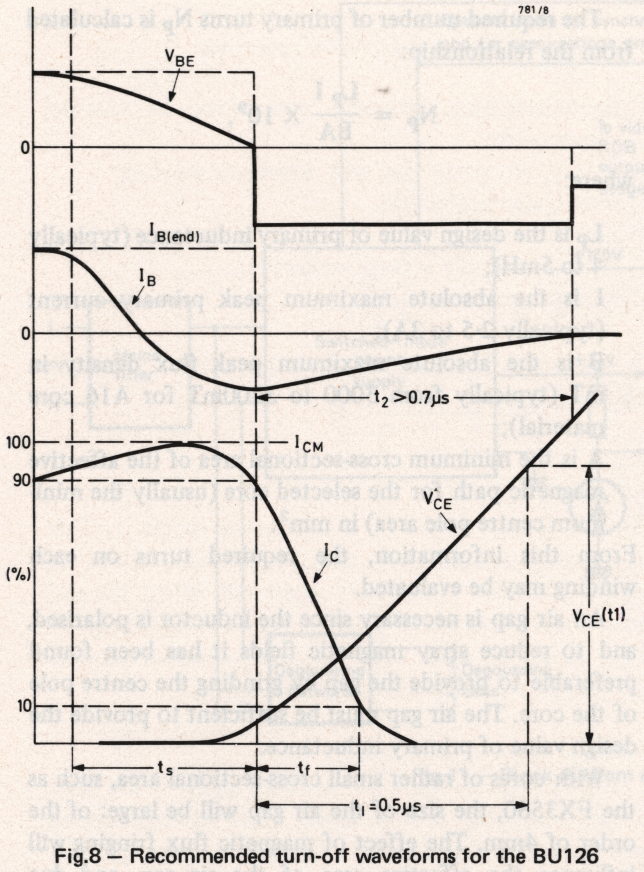

Fig.8 – Recommended turn-off waveforms for the BU126

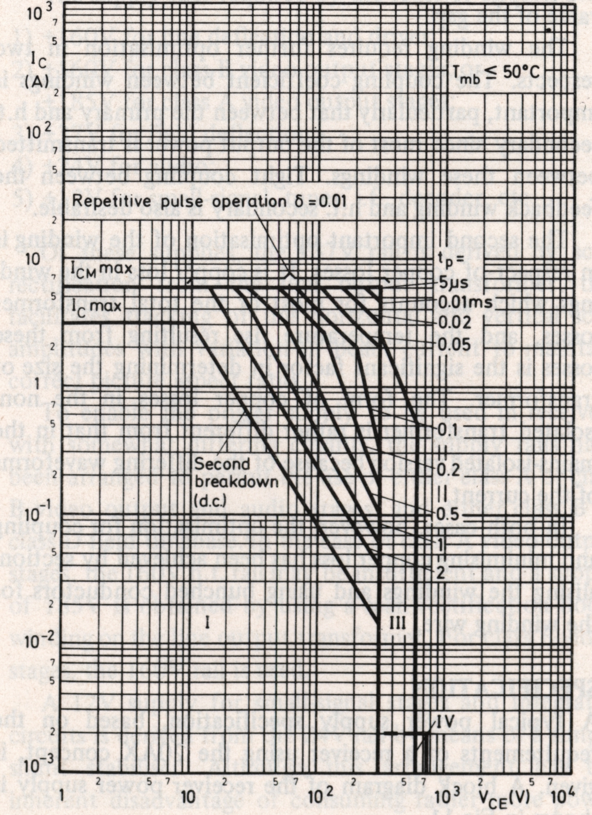

Fig.9 – Safe operating area of the BU126

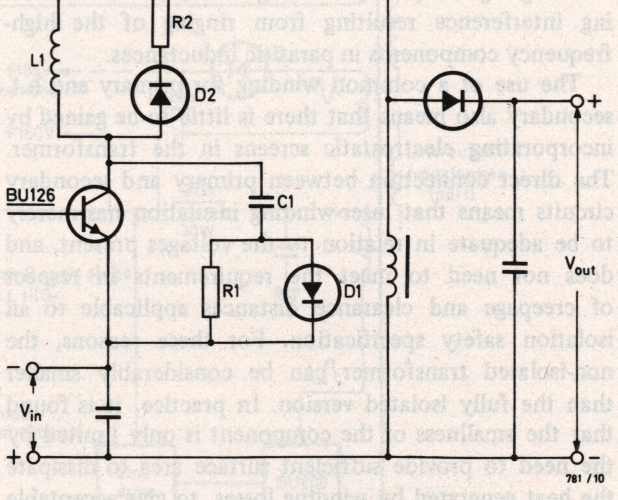

Fig.10 – Second-breakdown protection arrangements for choke-coupled SMPS

Output transformer

The two alternative versions of the power supply employ similar circuits for driver stage, control system, mains rectification, and filtering, as well as the BU126 power switching stage. It is in the area of the output transformer that the differences between the two versions arise.

Non-isolated transformer

In the non-isolated transformer, a single common winding serves for both primary and h.t. secondary. For this reason, the non-isolated output transformer is often referred to as a choke. Because the primary and h.t. secondary circuits are connected to a common winding, the problems due to coupling losses in the transformer are considerably eased. Furthermore, since the current supplied to the primary circuit is of a similar magnitude to the current supplied by the h.t. secondary circuit, and both are of trapezoidal waveform, the resultant current in the inductor consists largely of d.c. with a superimposed triangular ripple. This is advantageous in reducing high-frequency winding losses, and in minimising interference resulting from ringing of the high-frequency components in parasitic inductances.

The use of a common winding for primary and h.t. secondary also means that there is little to be gained by incorporating electrostatic screens in the transformer. The direct connection between primary and secondary circuits means that inter-winding insulation has merely to be adequate in relation to the voltages present, and does not need to meet the requirements in respect of creepage and clearance distances applicable to an isolation safety specification. For these reasons, the non-isolated transformer can be considerably smaller than the fully isolated version. In practice, it is found that the smallness of the component is only limited by the need to provide sufficient surface area to dissipate the heat generated by winding losses, to give acceptable temperature rise in the materials used in the construction of the transformer.

Mains-isolated transformer

Although the primary and secondary peak currents and voltages and the core flux excursion in the mains-isolated transformer are similar to those in the non-isolated transformer, there are two significant differences. The more conventional separate primary and h.t. secondary windings introduce a requirement for low leakage reactance between these windings, to maintain high efficiency. This can be achieved by sectionalising the two windings and winding with a large ratio of width to height.

The requirements of the safety regulations imply the need for a winding window size considerably in excess of the copper area, to provide the necessary creepage distances. Both of these factors, together with the need to incorporate screens between all primary and secondary interfaces, result in a substantially larger wound component than for the non-isolated case.

Design procedure

The technique adopted for both types of transformer is similar. The design of the power supply circuit requires that the output transformer has a certain minimum value of primary inductance, typically 4 to 5mH for this application at 16kHz. Since it is undesirable to make the inductance much higher than the designed minimum value, the lower limit of tolerance is made equal to the minimum figure.

Again, the circuit requirements will dictate an absolute maximum value of peak primary current (end-of-conduction current). All primary-to-secondary ratios are known and a value of peak flux density is determined in relation to acceptable core losses resulting from the alternating component of flux density.

The required number of primary turns N_P is calculated from the relationship:

$$N_P = \frac{L_P I}{BA} \times 10^9,$$

where:

L_P is the design value of primary inductance (typically 4 to 5mH);

I is the absolute maximum peak primary current (typically 2·5 to 3A);

B is the absolute maximum peak flux density in mT (typically from 3000 to 3200mT for A16 core material);

A is the minimum cross-sectional area of the affective magnetic path for the selected core (usually the minimum centre pole area) in mm^2.

From this information, the required turns on each winding may be evaluated.

An air gap is necessary since the inductor is polarised, and to reduce stray magnetic fields it has been found preferable to provide the gap by grinding the centre pole of the core. The air gap must be sufficient to provide the design value of primary inductance.

With cores of rather small cross-sectional area, such as the FX3560, the size of the air gap will be large: of the order of 4mm. The effect of magnetic flux fringing will influence the effective area of the air gap, and due allowance for this must be made in determining the final value of the gap.

The winding requires further optimisation in two respects. The coupling coefficient between windings is important, particularly that between the primary and h.t. secondary since most of the output power is transmitted between these windings. Tight coupling between the feedback winding and h.t. secondary is also desirable.

The second important optimisation of the winding is in respect of copper losses. It is copper loss in the windings which accounts for most of the total transformer losses, and the temperature rise resulting from these losses is the significant factor in determining the size of transformer. The form of copper losses in the non-isolated transformer is rather different from that in the mains-isolated version because of the differing waveforms of the current.

In both cases, however, the optimisation for coupling and minimising copper loss has been achieved by sectionalising the windings and using bunched conductors for the winding wire.

SPECIFICATION

A typical power supply specification, based on the requirements of a receiver using the 20AX concept, is given. A block diagram of the receiver power supply is shown in Fig.11.

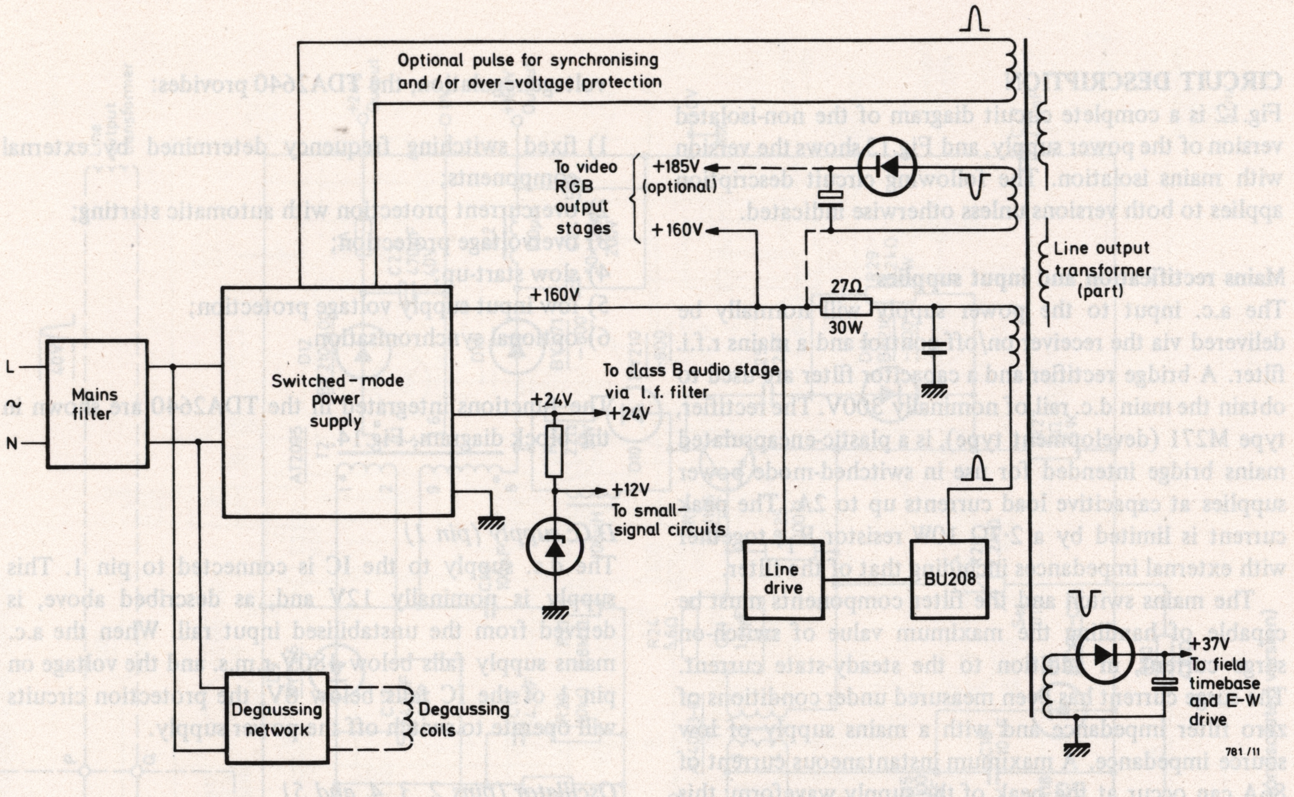

Fig.11 – Block diagram of complete receiver power supply

The supply rails required by the receiver circuits are:

1) +160V for line deflection and driver;
2) +160V for class B video output stages; or
   +185V for class A video output stages;
3) +37V for field deflection;
4) +24V for audio;
5) +12V for small-signal, tuner, i.f., decoder, etc.

Of these supplies, the +37V rail is derived by scan rectification from the line output transformer; this facilitates tracking of the horizontal and vertical scan amplitudes with variation in beam current to maintain correct picture aspect ratio.

To enable the power supply to be used in receivers with somewhat differing circuits, the supply rails have been arranged to permit the use of either class A or class B video output and audio stages, and either class B or class D field timebase. In the case of class A video output stages, the 160V h.t. rail may be insufficient and a supply of 185V is obtained by using a scan rectification boost winding on the line output transformer. For class B video stages, the 160V rail is used.

A 12V supply for small-signal stages and integrated circuits is derived from the 24V rail by means of a simple shunt stabiliser. Although this arrangement has the inherent disadvantage of consuming rather more power than could be achieved by directly generating a separate 12V supply, it has the advantage of keeping the supply voltage to the ICs constant, irrespective of any adjustment or variation in the setting of the power supply output voltages.

The total loading placed upon the power supply by a 20AX receiver can be as low as 130W (including beam current), where low-consumption circuits are employed. A more typical value would be 160W and therefore, to permit various optional receiver circuits, the power supply has been designed to accept an absolute maximum total loading of 180W.

The maximum load on each supply rail is shown in the following summarised specification.

A.C. mains input: min. 180V r.m.s.
max. 265V r.m.s.
H.T. output: 160V at 1A.
L.T. output: 24V at 700mA.
Minimum operating load: 80W.
Switching frequency of power supply: 16 to 20kHz (fixed within these limits).
Stabilisation: variation in h.t. (all causes) not to exceed ± 5%.
Ripple level: 50 and 100Hz hum < 300mV pk-pk, referred to h.t. output.
Protection circuits: overcurrent (preset level); overvoltage (preset level).

CIRCUIT DESCRIPTION

Fig.12 is a complete circuit diagram of the non-isolated version of the power supply, and Fig.13 shows the version with mains isolation. The following circuit description applies to both versions unless otherwise indicated.

Mains rectification and input supplies

The a.c. input to the power supply will normally be delivered via the receiver on/off control and a mains r.f.i. filter. A bridge rectifier and a capacitor filter are used to obtain the main d.c. rail of nominally 300V. The rectifier, type M271 (development type), is a plastic-encapsulated mains bridge intended for use in switched-mode power supplies at capacitive load currents up to 2A. The peak current is limited by a 2·7Ω 10W resistor R_1, together with external impedances including that of the filter.

The mains switch and the filter components must be capable of handling the maximum value of switch-on surge current, in addition to the steady-state current. The surge current has been measured under conditions of zero filter impedance and with a mains supply of low source impedance. A maximum instantaneous current of 86A can occur at the peak of the supply waveform; this corresponds to 6·5A averaged over 10ms, and an I^2t value of 3·7J/Ω.

The filter capacitor C_6 is a type intended for this application, with an appropriate ripple current rating and a working voltage up to 385V. A slow-acting fuse is incorporated in the mains side of the bridge rectifier, and a fast-acting fuse is in the supply to the output transistor. Over the range of a.c. input voltage from 180 to 265V r.m.s. the average d.c. supply rail voltage is approximately 225 to 345V. The peak-to-peak 100Hz ripple level is of the order of 25V, depending upon the loading and the input voltage.

The low-voltage supply rail of nominally 12V, for the control circuit, is derived through a dropping resistor R_2 from the 300V rail.

A regulator diode D_6, type BZY88-C12, prevents the 12V rail voltage from rising excessively at high mains voltage, whilst at low mains voltage this diode will be cut off.

A supply for the driver stage is also derived from the 300V rail; the diode D_5 (BYX94) and a 25μF capacitor provide a supply which has a lower ripple level and which decays more slowly than the supply to the output transistor when the mains supply is removed. Base current to the output transistor is thus maintained during switch-off.

Control circuit

The silicon monolithic integrated circuit type TDA2640 provides all the control functions. In addition to output voltage regulation, the TDA2640 provides:

1) fixed switching frequency determined by external components;
2) overcurrent protection with automatic starting;
3) overvoltage protection;
4) slow start-up;
5) low input supply voltage protection;
6) optional synchronisation.

The functions integrated in the TDA2640 are shown in the block diagram, Fig.14.

D.C. supply (pin 1)

The d.c. supply to the IC is connected to pin 1. This supply is nominally 12V and, as described above, is derived from the unstabilised input rail. When the a.c. mains supply falls below 180V r.m.s. and the voltage on pin 1 of the IC falls below 8V, the protection circuits will operate to switch off the power supply.

Oscillator (pins 2, 3, 4, and 5)

A Miller integrator type of oscillator is used: the free-running frequency is determined by an external timing network comprising capacitor C_{10} and resistor R_4. The oscillator may be synchronised to the horizontal scanning frequency by applying a positive pulse at pin 2. In this case, for satisfactory locking the timing components must place the free-running frequency somewhat higher than the synchronised frequency. Where synchronisation is not used, pin 2 should be connected to the common rail, pin 16.

Output (pin 6)

The pulse-width modulated output is obtained from pin 6. The output circuit within the IC uses an n-p-n transistor with a catching diode to the internal 12V rail. This gives a low output impedance in the 'on' state, that is with the driver transistor turned off.

Low feedback protection (pin 7)

An 82kΩ resistor connected from pin 7 to pin 13 determines the shape of the transfer characteristic in the region where the level of feedback voltage on pin 10 is outside defined limits.

If the normal operation of the control loop is interrupted by a loss of voltage on pin 10, then the duty cycle will assume a low value of about 15%; without this protection it would settle at the maximum value. It should be noted that a failure in the feedback rectification circuit, for example, will not normally cause this circuit to operate because of the presence of resistor R_{11} between pins 9 and 10.

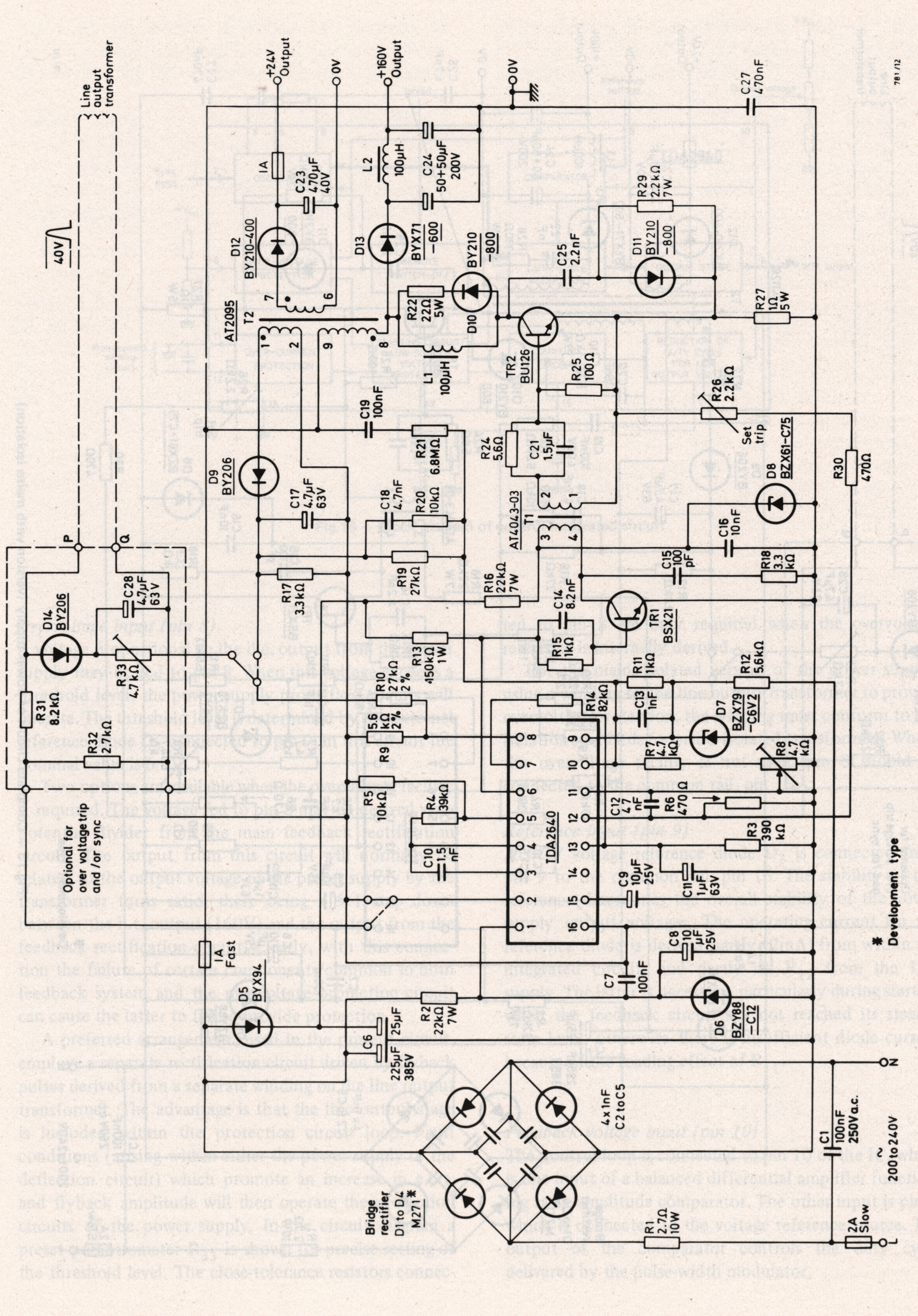
+24V Output
0V
+160V Output
0V
Line output transformer
40V
P
Q
Optional for over voltage trip and/or sync
D14 BY206
C28 4.7µF 63V
R33 4.7kΩ
R31 8.2kΩ
R32 2.7kΩ
D12 BY210-400
1A
C23 470µF 40V
AT2095
T2
D13 BYX71-600
L2 100µH
C24 50+50µF 200V
BY210-800
D10
R22 22Ω 5W
L1 100µH
C19 100nF
D9 BY206
C17 47µF 63V
R17 3.3kΩ
R19 27kΩ
C18 4.7nF
R20 10kΩ
R21 6.8MΩ
TR2 BU126
C25 2.2nF
D11 BY210-800
R29 2.2kΩ 7W
C27 470nF
R27 1Ω 5W
R25 100Ω
R24 5.6Ω
C21 1.5µF
AT4043-03 T1
R26 2.2kΩ
Set trip
D8 BZX61-C75
R30 470Ω
R16 22kΩ 7W
C14 8.2nF
TR1 BSX21
C15 100pF
C16 10nF
R18 3.3kΩ
R15 1kΩ
R13 150kΩ 1W
R10 2.7kΩ 2%
R9 5.6kΩ 2%
R14 82kΩ
C13 1nF
R11 1kΩ
R12 5.6kΩ
D7 BZX79-C6V2
R7 4.7kΩ
R8 4.7kΩ
R5 10kΩ
R4 39kΩ
TDA2640
C12 4.7nF
R6 470Ω
R3 390kΩ
C10 1.5nF
C9 10µF 25V
C11 1µF 63V
1A Fast
D5 BYX94
C8 10µF 25V
C7 100nF
D6 BZY88-C12
C6 225µF 385V
R2 22kΩ 7W
Bridge rectifier D1 to D4 M271✱
4x1nF C2 to C5
R1 2.7Ω 10W
C1 100nF 250V a.c.
2A Slow
200 to 240V
N
L
781/12

Fig.12 — Complete circuit of power supply (non-isolated version)

✱ Development type

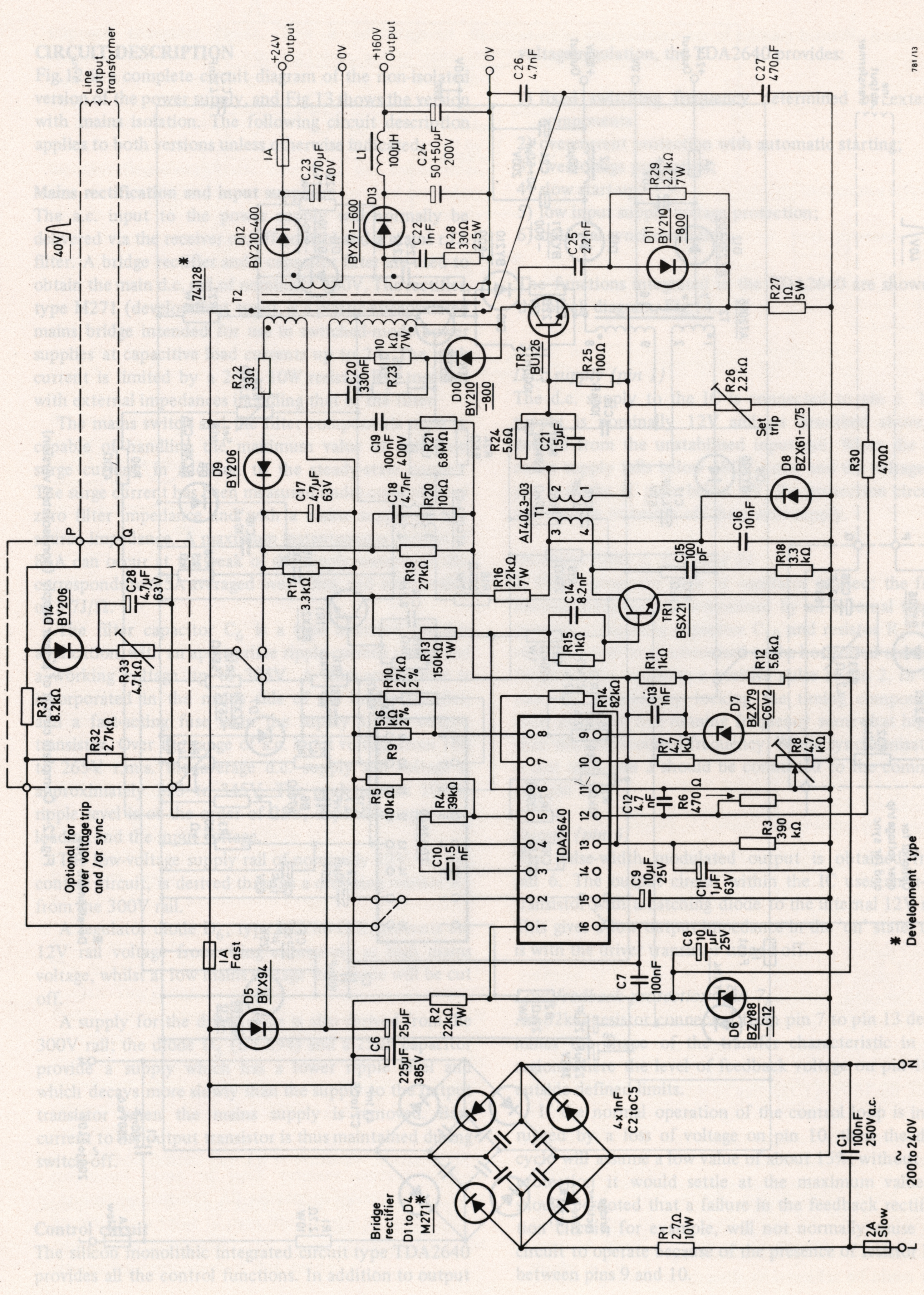
Line output transformer
+24V Output
0V
+160V Output
0V
C26 4.7nF
C27 470nF
1A
C23 470µF 40V
L1 100µH
C24 50+50µF 200V
D12 BY210-400
D13 BYX71-600
C22 1nF
R28 330Ω 2.5W
R29 2.2kΩ 7W
D11 BY210 -800
C25 2.2nF
R27 1Ω 5W
40V
AT4128
T2
R22 33Ω
C20 330nF
R23 10 kΩ 7W
D10 BY210 -800
TR2 BU126
R25 100Ω
R26 2.2kΩ
Set trip
C19 100nF 400V
R21 6.8MΩ
R24 56Ω
C21 1.5µF
D8 BZX61-C75
R30 470Ω
D9 BY206
C17 4.7µF 63V
C18 4.7nF
R20 10kΩ
AT4043-03
T1
C16 10nF
C15 100 pF
R18 3.3 kΩ
P
Q
C28 4.7µF 63V
R17 3.3kΩ
R19 27kΩ
R16 22kΩ 7W
C14 8.2nF
TR1 BSX21
D14 BY206
R33 4.7kΩ
R10 27kΩ 2%
R13 150kΩ 1W
R15 1kΩ
R11 1kΩ
R12 5.6kΩ
R31 8.2kΩ
R32 2.7kΩ
5.6 kΩ 2%
R9
R14 82kΩ
C13 1nF
D7 BZX79 -C6V2
R7 4.7 kΩ
R8 4.7 kΩ
R5 10kΩ
R4 39kΩ
TDA2640
C12 47 nF
R6 470 Ω
R3 390 kΩ
C10 1.5 nF
C9 10µF 25V
C11 1µF 63V
Optional for over voltage trip and /or sync
C8 10 µF 25V
C7 100nF
1A Fast
D5 BYX94
C6 225µF 385V
25µF
R2 22kΩ 7W
D6 BZY88 -C12
N
L
4×1nF C2 to C5
C1 100nF 250V a.c.
~ 200 to 240V
Bridge rectifier D1 to D4 M271
R1 2.7Ω 10W
2A Slow
* Development type
781/13

Fig.13 — Complete circuit of power supply (version with mains isolation)

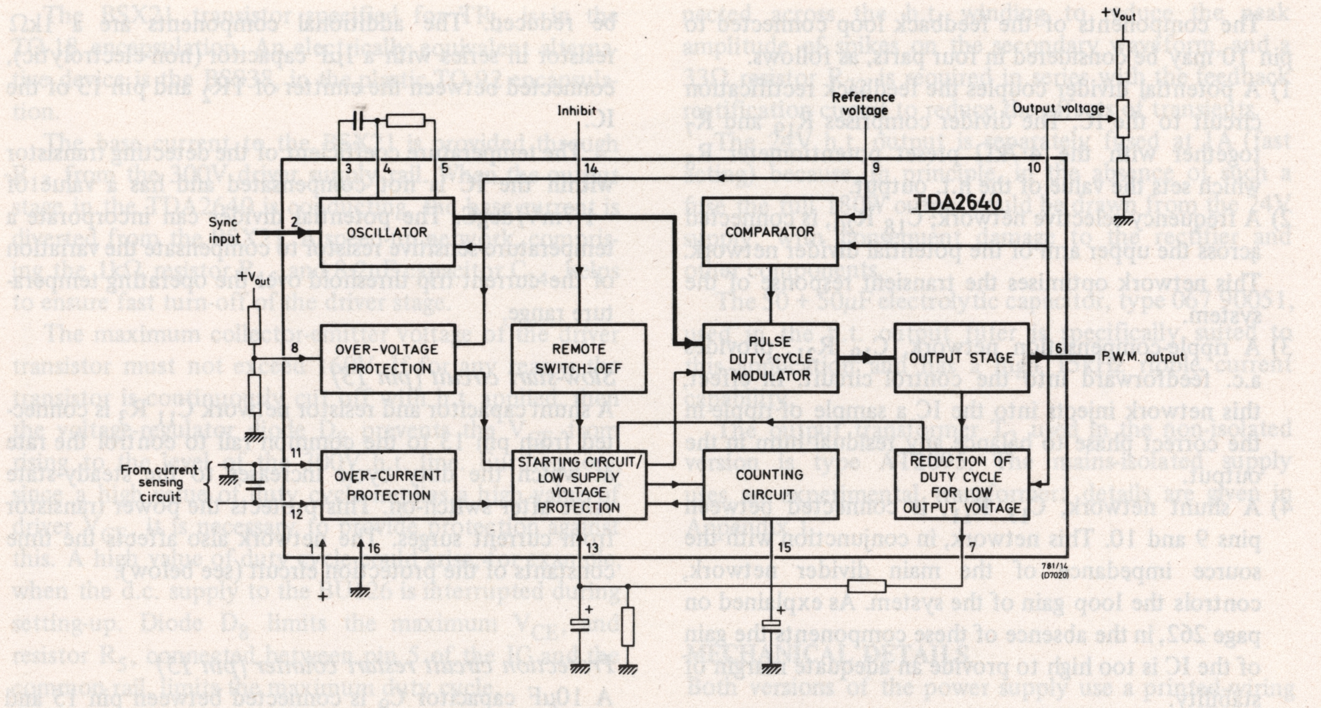
+Vout
Inhibit
Reference voltage
Output voltage
Sync input
+Vout
OSCILLATOR
COMPARATOR
TDA2640
OVER-VOLTAGE PROTECTION
REMOTE SWITCH-OFF
PULSE DUTY CYCLE MODULATOR
OUTPUT STAGE
P.W.M. output
From current sensing circuit
OVER-CURRENT PROTECTION
STARTING CIRCUIT/ LOW SUPPLY VOLTAGE PROTECTION
COUNTING CIRCUIT
REDUCTION OF DUTY CYCLE FOR LOW OUTPUT VOLTAGE
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
781/14 (D7020)

Fig.14 — Block diagram of control integrated circuit

Overvoltage input (pin 8)

A voltage proportional to the d.c. output from the power supply may be fed to pin 8. When this voltage exceeds a threshold level, the power supply protection circuits will operate. The threshold level is determined by the external reference diode D_7 connected to pin 9; in this circuit the nominal value is 6·2V.

Two options are available when the overvoltage facility is required. The voltage fed to pin 8 may be derived via a potential divider from the main feedback rectification circuit. The output from this circuit will normally be related to the output voltage of the power supply by the transformer turns ratio, there being a 5:1 step down between the h.t. output (160V) and the output from the feedback rectification circuit. Clearly, with this connection the failure of certain components common to both feedback system and the overvoltage protection circuit can cause the latter to fail to provide protection.

A preferred arrangement, used in the present circuit, employs a separate rectification circuit driven by flyback pulses derived from a separate winding on the line output transformer. The advantage is that the line output stage is included within the protection circuit loop. Fault conditions (arising within either the power supply or the deflection circuit) which promote an increase in e.h.t. and flyback amplitude will then operate the protection circuits of the power supply. In the circuit diagram a preset potentiometer R_{33} is shown for precise setting of the threshold level. The close-tolerance resistors connected to pin 8 are only required when the overvoltage reference is internally derived.

For the mains-isolated version of the power supply, using a winding on the line output transformer to provide overvoltage protection, the winding must conform to the isolation standards for mains-isolated transformers. Where the overvoltage facility is not used, pin 8 should be connected to the common rail, pin 16.

Reference input (pin 9)

A 6·2V voltage reference diode D_7 is connected from pin 9 to the common rail, pin 16. The stability of this reference determines the overall stability of the power supply output voltages. The operating current for the reference diode is derived partly (2mA) from within the integrated circuit, and partly via R_{12} from the 12V supply. The latter is necessary, particularly during starting when the feedback circuit has not reached its steady-state level, otherwise there is insufficient diode current because of the loading effect of R_{11}.

Feedback voltage input (pin 10)

The control loop is connected to pin 10 of the IC, which is one input of a balanced differential amplifier functioning as an amplitude comparator. The other input is pin 9, which is connected to the voltage reference source. The output of the comparator controls the duty cycle delivered by the pulse-width modulator.

The components of the feedback loop connected to pin 10 may be considered in four parts, as follows.

1) A potential divider couples the feedback rectification circuit to the IC. The divider comprises R_{19} and R_7 together with the 4·7kΩ preset potentiometer R_8 which sets the value of the h.t. output.
2) A frequency-selective network, C_{18} R_{20}, is connected across the upper arm of the potential divider network. This network optimises the transient response of the system.
3) A ripple-compensation network, C_{19} R_{21}, provides a.c. feedforward into the control circuit. In effect, this network injects into the IC a sample of ripple in the correct phase to balance any residual hum in the output.
4) A shunt network, C_{13} R_{11}, is connected between pins 9 and 10. This network, in conjunction with the source impedance of the main divider network, controls the loop gain of the system. As explained on page 262, in the absence of these components the gain of the IC is too high to provide an adequate margin of stability.

Overcurrent input (pins 11 and 12)

A voltage proportional to the current in the output transistor TR_2 is applied between pins 11 and 12. Pin 11 is the emitter of the detecting transistor and pin 12 is the base. The current in the output transistor is sampled by a 1Ω resistor R_{27} in the emitter circuit. A potential divider, incorporating a preset resistor R_{26} for adjusting the current trip threshold, feeds part of the voltage developed across R_{27} to pin 12 of the IC. Pin 11 is connected to the common rail (pin 16) in this case, because the applied voltage is positive-going for increasing current in TR_2. When the voltage between pins 11 and 12 exceeds typically 700mV, the protection circuits will operate.

A small capacitor C_{12} is connected directly between pins 11 and 12 to prevent premature operation of the protection circuit due to interference spikes. The value of this capacitor must not be too large, or else the delay produced in the circuit may lead to excessive peak current in TR_2, particularly if the power supply is turned on with a short-circuited output.

The current trip is normally adjusted to operate at a point somewhat above the level at which the power supply operates when delivering maximum output (180W) at minimum a.c. input (180V r.m.s.).

Where the maximum loading is significantly less than 180W, it is impracticable simply to reduce the current trip threshold because the start-up current may cause permanent tripping. It is possible, however, to reduce the start-up current by adding components to the circuit; if this is done then the current trip threshold can safely be reduced. The additional components are a 1kΩ resistor in series with a 1μF capacitor (non-electrolytic), connected between the emitter of TR_2 and pin 13 of the IC.

The temperature coefficient of the detecting transistor within the IC is not compensated and has a value of −1·7mV/degC. The potential divider can incorporate a temperature-sensitive resistor to compensate the variation of the current trip threshold over the operating temperature range.

Slow-start circuit (pin 13)

A shunt capacitor and resistor network C_{11} R_3 is connected from pin 13 to the common rail to control the rate at which the duty cycle increases to the steady-state value after switch-on. This protects the power transistor from current surges. The network also affects the time constants of the protection circuit (see below).

Protection circuit restart counter (pin 15)

A 10μF capacitor C_9 is connected between pin 15 and the common rail to control the characteristics of the protection circuits.

If either of the protection circuits is activated, then the duty cycle will be set to zero, turning off the power supply. After a short interval (determined by the time-constant on pin 13) the power supply will be restarted via the slow-start circuit. If the fault condition has cleared, then normal operation will be resumed. If the fault persists, the shut-down and restart cycle will be repeated. The number of times this action is repeated for a persisting fault condition is determined by a counting circuit within the IC, controlled by C_9.

Remote control input (pin 14)

The IC incorporates facilities for remote control. By applying an appropriate d.c. level to pin 14, the power supply can be turned on and off. When the voltage is high (5 to 12V) or the pin is floating, the power supply operates normally; when the voltage is low (0 to 3V), the power supply is inhibited. The slow-start and protection circuits are all operative with remote control.

The present power supply design, however, does not make use of this facility. If remote control of this power supply is required, then the control signal must be fed to the IC through an isolating circuit, such as a photocoupler.

Driver stage

The driver stage employs a BSX21 transistor TR_1 in a transformer-coupled circuit. The design follows the principles previously outlined.

The BSX21 transistor specified for TR_1 is in the TO-18 encapsulation. An electrically equivalent alternative device is the BSS38, in the plastic TO-92 encapsulation.

The base current to the BSX21 is provided through R_{13} from the 300V driver supply rail. When the output stage in the TDA2640 is conducting, the base current is diverted from the BSX21. A speed-up network, comprising the 1kΩ resistor R_{15} and 8·2nF capacitor C_{14}, helps to ensure fast turn-off of the driver stage.

The maximum collector-emitter voltage of the driver transistor must not exceed 160V. If for any reason the transistor is continuously cut off with h.t. applied, then the voltage-regulator diode D_8 prevents the V_{CE} from rising to the level of the 300V h.t. line. Furthermore, since a high value of duty cycle implies a high value of driver V_{CE}, it is necessary to provide protection against this. A high value of duty cycle could arise, for example, when the d.c. supply to the BU126 is interrupted during setting-up. Diode D_8 limits the maximum V_{CE}, and resistor R_5, connected between pin 5 of the IC and the common rail, limits the maximum duty cycle.

The forward characteristic of the regulator diode D_8 prevents spurious drive pulses from being fed to the BU126 as a result of circuit resonances in the driver stage, as previously described.

The driver transformer T_1, type AT4043-03, is designed specifically for non-simultaneous operation in this application.

The optimum base current for the BU126 is as indicated in Fig.6. The 22kΩ resistor R_{16} in the h.t. supply to the driver transistor controls the base current to the BU126. The value of this resistor is appropriate when the power supply loading is near its rated maximum of 180W. For an application where a lower maximum load will be imposed, the value of R_{16} may be increased to bring the base current into line with the recommendation for the corresponding value of 'end-of-conduction' collector current in the BU126 output transistor.

Output stage

To limit the maximum rate of rise of the BU126 collector-emitter voltage, a network comprising a 2·2nF capacitor C_{25}, a 2·2kΩ resistor R_{29}, and a diode type BY210 is connected across the transistor.

The non-isolated version of the power supply (Fig.12) includes an inductor L_1 of 100μH with a damping resistor and diode, connected in series with the collector circuit of TR_2 to reduce the turn-on dissipation. The mains-isolated version does not require this inductance, because the transformer leakage inductance has the same effect. However, a damping network C_{20} R_{23} D_{10} is now required across the primary winding of the transformer. In addition, a further damping network C_{22} R_{28} is connected across the h.t. winding to reduce the peak amplitude of spikes on the secondary waveform, and a 33Ω resistor R_{22} is required in series with the feedback rectification circuit to reduce the effects of transients.

The 24V h.t. output is separately fused at 1A (fast acting) because, in principle, in the absence of such a fuse the full 180W output could be drawn from the 24V supply, with consequent damage to the rectifier and other components.

The 50 + 50μF electrolytic capacitor, type 067 90051, used in the h.t. output filter is specifically suited to this application and has a high 15kHz ripple current capability.

The output transformer T_2 used in the non-isolated version is type AT2095. The mains-isolated supply uses an experimental transformer: details are given in Appendix 1.

MECHANICAL DETAILS

Both versions of the power supply use a printed-wiring board with overall dimensions 225 × 130mm; the maximum height is 60mm. The component layout of the non-isolated version is shown in Fig.15, and the layout of the isolated version is similar. Fig.16 is a photograph of a prototype non-isolated power supply.

The output transistor and the BYX71 rectifier must be mounted on heatsinks. A single heatsink is used for both, with the devices well separated from each other and mounted with mica washers. The heatsink is a piece of 1mm blackened aluminium, approximately 225 × 80mm.

Certain precautions are necessary in the layout of switched-mode power supplies: some of the significant points are summarised below.

The printed tracks for the input supply must be adequately rated to carry the maximum input surge current. The various points of the circuit fed from the input supply should be connected together directly at the terminals of the 225μF electrolytic capacitor. This is particularly important for the supply to the output transistor TR_2. An additional 470nF capacitor is connected across the supply as close as possible to TR_2 and the transformer primary.

A similar scheme should be adopted for the main h.t. output electrolytic capacitor. In general, earth loops and common impedances should be avoided.

The TDA2640 integrated circuit and its peripherals should be well separated from high-voltage circuits such as the output and driver stages, and from the 50Hz circuits. On small boards it may be more convenient to enclose the control circuits in a screening can.

Prototype versions of both supplies have been enclosed in perforated aluminium screening boxes.

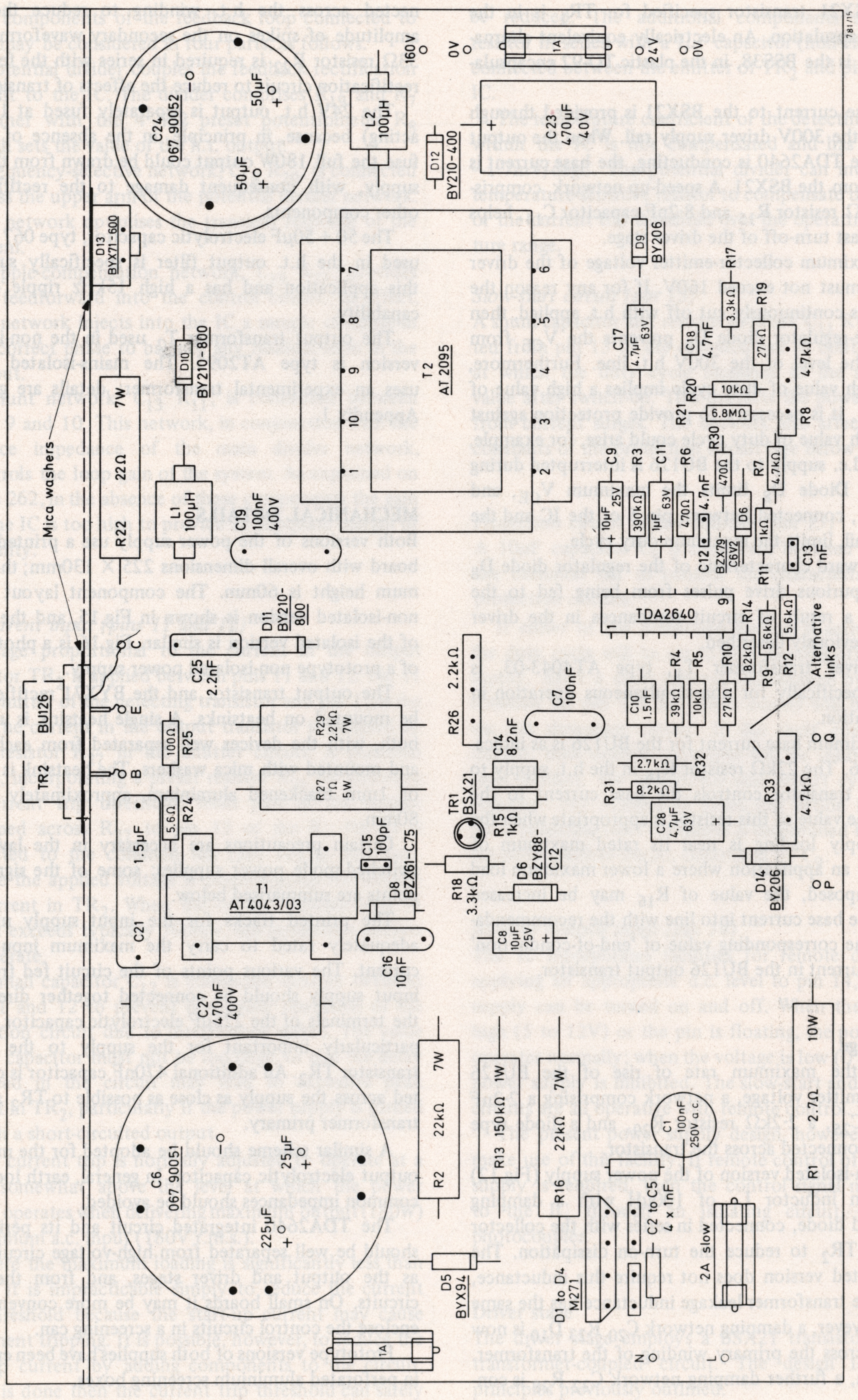
Mica washers
BU126
TR2
C24 067 90052
50µF
L2 100µH
160V
0V
24V
0V
1A
C23 470µF 40V
D12 BY210-400
D13 BYX71-600
D9 BY206
R17
R19 3.3kΩ
T2 AT 2095
C17 4.7µF 63V
C18 4.7nF
27kΩ
R20 10kΩ
R21 6.8MΩ
R8 4.7kΩ
D10 BY210-800
7W
22Ω
R22
L1 100µH
C19 100nF 400V
D11 BY210-800
C25 2.2nF
R29 2.2kΩ 7W
R25 100Ω
R24 5.6Ω
R27 1Ω 5W
C21 1.5µF
T1 AT4043/03
C15 100pF
D8 BZX61-C75
C16 10nF
C27 470nF 400V
C6 067 90051
25µF
225µF
D5 BYX94
R2 22kΩ 7W
R13 150kΩ 1W
R16 22kΩ 7W
C1 100nF 250V a.c.
C2 to C5 4 x 1nF
2A slow
D1 to D4
R1 2.7Ω 10W
N
L
1A
TDA2640
R26 2.2kΩ
C7 100nF
C14 8.2nF
TR1 BSX21
R15 1kΩ
D7 BZY88-C12
R18 3.3kΩ
C8 10µF 25V
R31 8.2kΩ
2.7kΩ
R32
C28 4.7µF 63V
R33 4.7kΩ
D14 BY206
C10 1.5nF
R4 39kΩ
R5 10kΩ
R10 27kΩ
82kΩ
R9 5.6kΩ
R14 5.6kΩ
R12 5.6kΩ
Alternative links
C9 10µF 25V
R3 390kΩ
C11 1µF 63V
R6 470Ω
C12 4.7nF
R30 470Ω
R7 4.7kΩ
D6 BZX79-C6V2
R11 1kΩ
C13 1nF

Fig.15 – Layout of non-isolated power supply on printed-wiring board. The layout of the mains-isolated version is similar

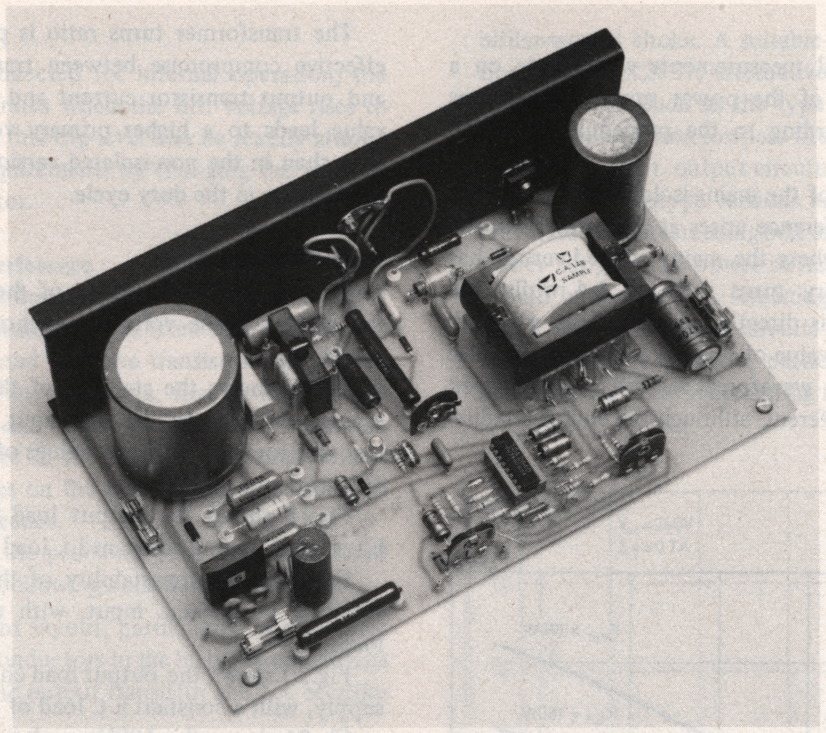

Fig.16 – Prototype television switched-mode power supply (version without mains isolation)

SETTING-UP PROCEDURE

The following procedure for setting-up and testing the power supply is suggested.

1) Connect load resistors to the output terminals.
   H.T. load: 160Ω, 160W.
   L.T. load: 34Ω, 20W.
   Link together the negative terminals of the h.t. and l.t. outputs. (The l.t. is a floating supply normally intended to be 'grounded' elsewhere in the receiver to avoid earth loops and common impedances.)
2) Link overvoltage protection circuit for internal operation.
3) Remove h.t. input fuse.
4) Apply an input supply of 240V r.m.s. and check the following d.c. voltages with respect to the common negative rail of the power supply, that is, the negative terminal of the input electrolytic capacitor C_6:
   C_6 (225µF section) positive terminal: +330V,
   C_6 (25µF section) positive terminal: +330V,
   D_6 cathode: +12V,
   D_7 cathode: +6·2V,
   Junction of R_{16} and T_1: +70V approx.
5) With an oscilloscope current probe examine the base current waveform of TR_2 and check the following:
   (a) frequency within the range 18 to 20kHz,
   (b) $+I_{B(pk)}$ (including overshoot) 700mA approx.,
   (c) $+I_{B(end)}$ 300mA approx.,
   (d) $-I_{B(pk)}$ 1A approx.
6) Check the slow-start circuit: switch off, pause, and switch on; check that the duty cycle increases slowly from an initial low value.
7) With power switched off, set the h.t. potentiometer R_8 to minimum h.t. (that is, maximum resistance in circuit), and initially set the current trip potentiometer R_{26} to approximately the mid-position. Fit a 1A fast-acting h.t. input fuse to apply power to TR_2 and switch on.
8) Adjust the h.t. to 160V. Check that the l.t. output is 24V.
9) Set the current trip threshold, as follows. Reduce the a.c. input voltage to the required minimum operating voltage (but not less than 180V r.m.s.). Reduce the setting of the current trip potentiometer (that is, reduce the resistance in circuit) until the power supply commences to trip, and then increase the setting to just above the point where tripping occurs. Switch the a.c. input off and then on again, to check that the power supply restarts without tripping, and if necessary make final adjustments to the setting.
10) At this stage it is desirable to examine the TR_2 collector current waveform and collector voltage of a prototype unit, to ascertain satisfactory operation.
11) Reduce the h.t. load to about 130W, retaining the l.t. load at about 20W. Increase the setting of the h.t. potentiometer, and check that the overvoltage protection circuit operates when the h.t. reaches about 180V.

PERFORMANCE

The following typical measurements were made on a non-isolated version of the power supply, which was initially set up according to the procedure described above.

The performance of the mains-isolated unit is similar; the most notable difference arises at the primary of the output transformer where the mains-isolated version has a primary-to-secondary turns ratio of 1·4 whilst the non-isolated version is directly coupled. This, together with a slightly lower value of primary inductance, makes the primary current waveform on the mains-isolated version somewhat different, although the end-of-conduction current is similar.

The transformer turns ratio is chosen to achieve an effective compromise between transformer inductance and output transistor current and voltage. The chosen value leads to a higher primary voltage and transistor V_{CE} than in the non-isolated version, and a corresponding increase in the duty cycle.

Regulation and ripple

The regulation performance of the power supply, and the output ripple voltage, are shown in the graphs of Figs.17 to 22.

Fig.17 shows the stability of the h.t. output supply against variation in the a.c. input, with a constant l.t. load and for three different values of total power output: 100, 160, and 180W.

Fig.18 shows the output load characteristic of the h.t. supply, with a constant l.t. load of 700mA.

Fig.19 shows the stability of the l.t. output against variation in the a.c. input, with constant h.t. and l.t. loads.

Fig.20 shows the output load characteristic of the l.t. supply, with a constant h.t. load of 1A.

Fig.21 shows the 100Hz peak-to-peak ripple level on the h.t. supply as a function of the h.t. load, with a constant l.t. load of 700mA.

Fig.22 shows the 100Hz peak-to-peak ripple level on the h.t. supply as a function of the a.c. input voltage, with an h.t. load of 1·015A and an l.t. load of 700mA (total power output 180W).

Minimum load

The minimum total load on the power supply should not normally be less than approximately 35W. Smaller loads will cause no danger, but the power supply switching frequency will be periodically interrupted as the control circuit stabilises the output voltage, producing an audible note in the wound components.

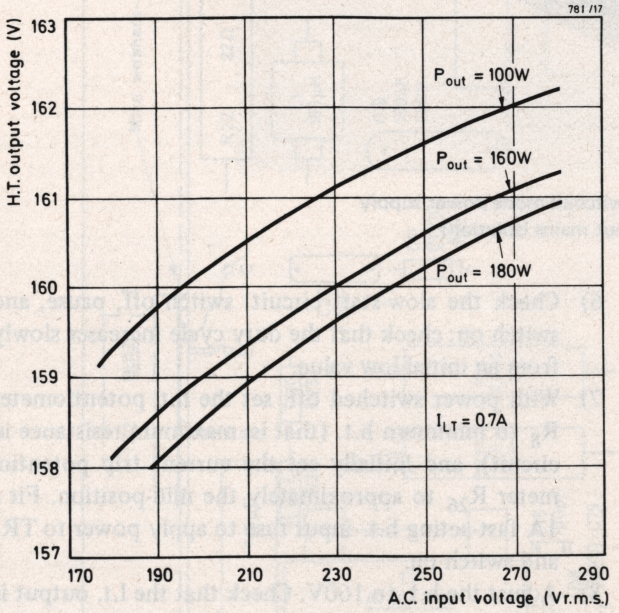

Fig.17 — H.T. output voltage as a function of a.c. input voltage

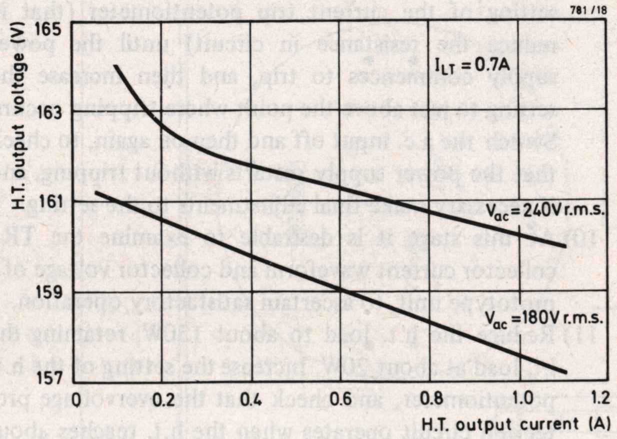

Fig.18 — H.T. output voltage as a function of h.t. load current

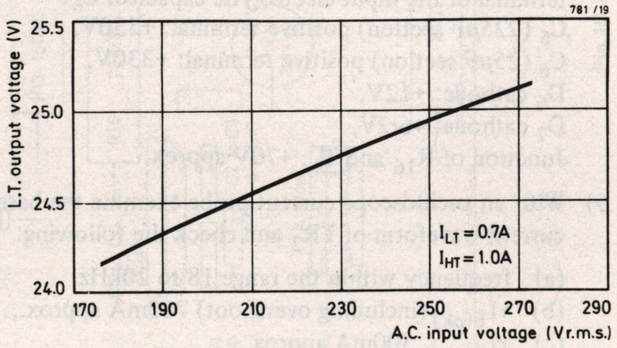

Fig.19 — L.T. output voltage as a function of a.c. input voltage

Overvoltage trip level

With the circuit connected for internal operation, the overvoltage trip operates when the h.t. voltage rises to 180V. The setting of this trip level may be readily altered to suit any other requirement, by changing the value of the appropriate resistor.

Radio-frequency interference

A switched-mode power supply is potentially a major source of r.f.i. The problem arises from the rapid switching transients associated with the transistors and diodes, and manifests itself in two ways; first as interference fed back into the a.c. mains supply, and second as interference elsewhere in the receiver, resulting perhaps in visible disturbances on the picture tube and radiation from the aerial and feeder.

In general terms, the problems of r.f.i. are minimised in this design by the following considerations.

1) Careful component layout, particularly in respect of using very short conductors in the high-current circuits associated with the output transistor and h.t. rectifier diode, etc.
2) Avoiding the use of diodes with 'snap-off' characteristics. All fast diodes in this power supply are soft recovery types, specifically designed to minimise interference. In cases where severe r.f.i. problems are encountered, it may be useful to connect low-value ceramic capacitors across fast diodes such as in the h.t. and l.t. circuits, preferably with a resistance in series (the effect of this capacitance upon the BU126 collector current must be carefully observed).
3) Including filter networks in input and output lines. A mains filter will normally be required in the input, to reduce interference on the mains supply to an acceptably low level. This filter may use a ferrite-cored bifilar-wound choke. A suitable core for this application is the FX2527; alternatively, a complete mains filter network such as the type MF2A may be used. Additional π-section lowpass filters may be connected in the h.t. and l.t. output circuits.
4) Screening. Prototype versions have been fitted with a perforated metal screening box enclosing the complete power supply. The power switching circuits, at least, should be screened. A screening box common to the SMPS power switching circuits and the tv deflection circuits may be possible, particularly if the SMPS is synchronised with the scanning frequency.

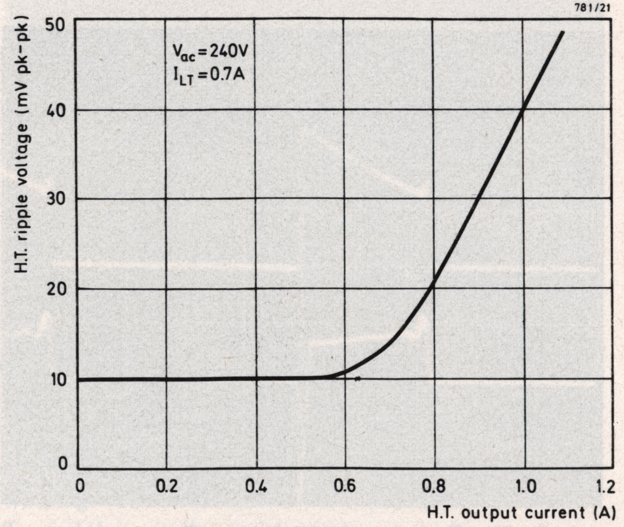

Fig.21 — H.T. output ripple voltage as a function of load current

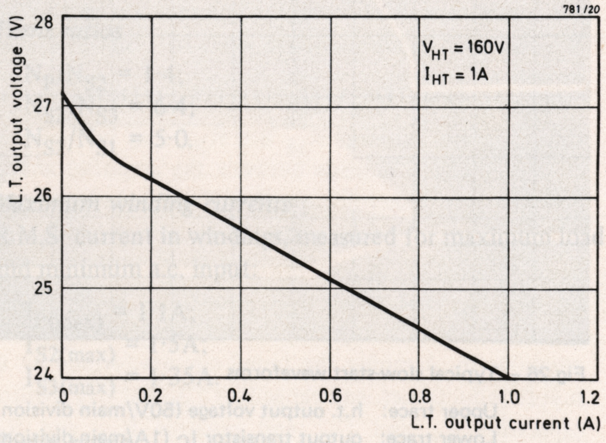

Fig.20 — L.T. output voltage as a function of l.t. load current

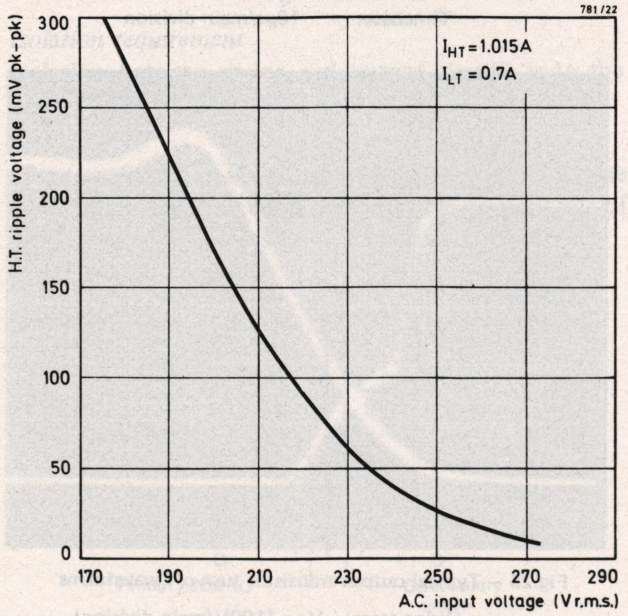

Fig.22 — H.T. output ripple voltage as a function of a.c. input voltage

Typical waveforms

Figs.23 to 27 show typical power supply waveforms measured on a prototype non-isolated power supply. The mains input voltage was 240V r.m.s. and the circuit was delivering the maximum output power of 180W.

The collector and base current waveforms of the output transistor are shown in Fig.23, and the collector current and voltage waveforms in Fig.24. Fig.25 shows, on an enlarged scale, the collector current and voltage waveforms at the instant of turn-off.

The operation of the slow-start circuit is shown in Fig.26: the upper trace shows the h.t. output voltage at switch-on, and the lower trace the output transistor collector current.

Fig.27 shows the effect on the output transistor collector current of short-circuiting the h.t. output.

Summary of operating conditions

Non-isolated power supply, switching frequency synchronised to 15·625kHz.

Output (maximum load)

H.T. output: 160V at 1·02A = 163W.
L.T. output: 24V at 700mA = 17W.
Total: 180W.

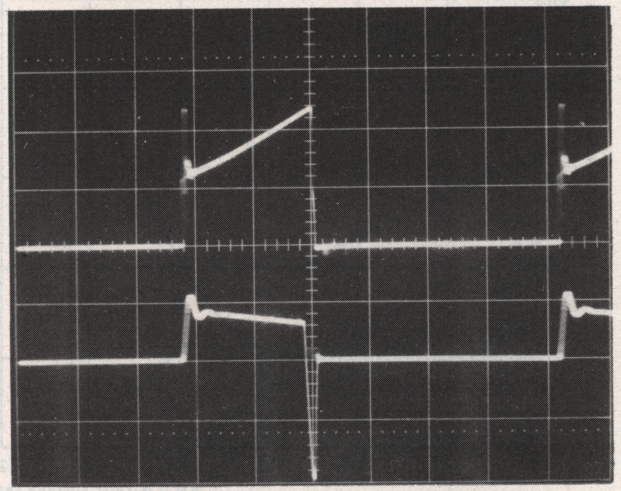

Fig.23 – Typical output transistor collector and base current waveforms

Upper trace: I_C (1A/main division)
Lower trace: I_B (0·5A/main division)
Timebase: 10μs/main division

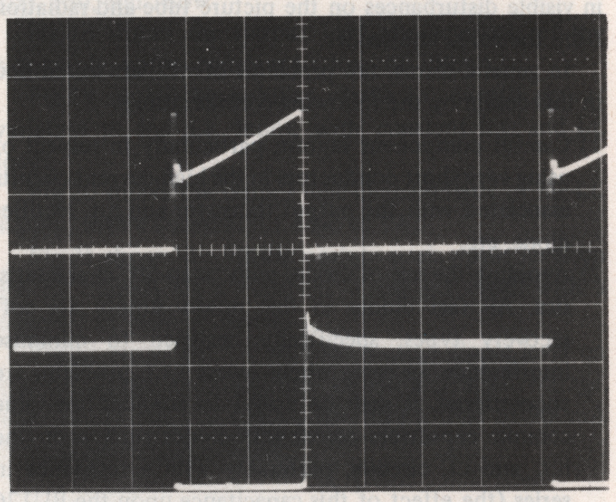

Fig.24 – Typical output transistor collector current and voltage waveforms

Upper trace: I_C (1A/main division)
Lower trace: V_{CE} (200V/main division)
Timebase: 10μs/main division

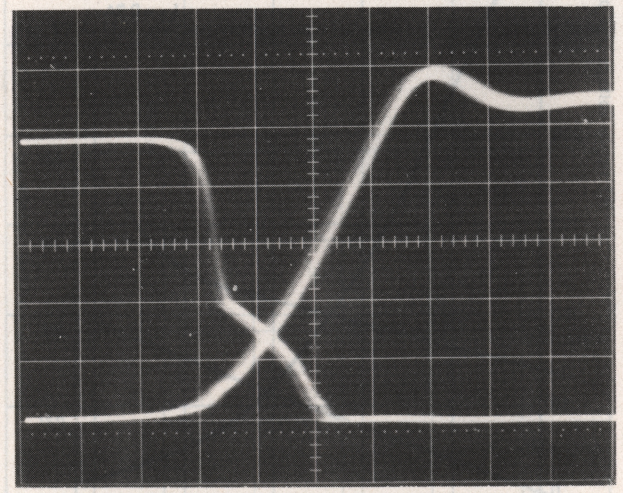

Fig.25 – Typical output transistor turn-off waveforms

Rising trace: V_{CE} (100V/main division)
Falling trace: I_C (0·5A/main division)
Timebase: 200ns/main division

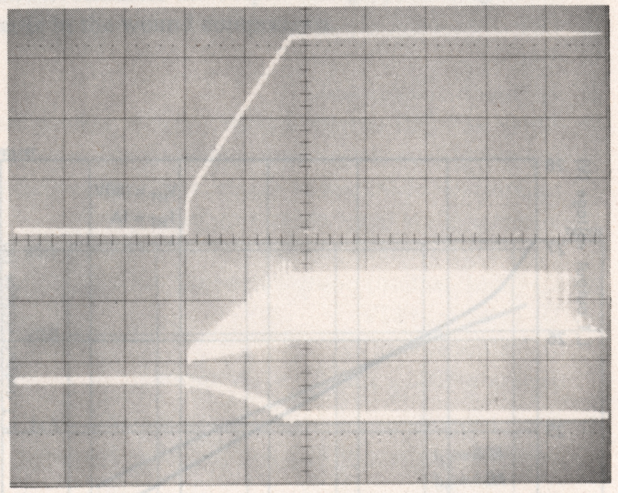

Fig.26 – Typical slow-start waveforms

Upper trace: h.t. output voltage (50V/main division)
Lower trace: output transistor I_C (1A/main division)
Timebase: 100ms/main division

Operating conditions of output transistor

1) At nominal input voltage, V_{ac} = 240V r.m.s.
$I_{C(end)}$ = 2·4A,
$V_{CE(pk)}$ = 580V,
$+I_{B(end)}$ = 320mA,
$-I_{B(pk)}$ = 1·0A.

2) At low input voltage, V_{ac} = 180V r.m.s.
$I_{C(end)}$ = 2·6A,
$V_{CE(pk)}$ = 510V,
$+I_{B(end)}$ = 240mA,
$-I_{B(pk)}$ = 0·81A.

3) At high input voltage, V_{ac} = 265V r.m.s.
$I_{C(end)}$ = 2·4A,
$V_{CE(pk)}$ = 625V,
$+I_{B(end)}$ = 340mA,
$-I_{B(pk)}$ = 1·04A.

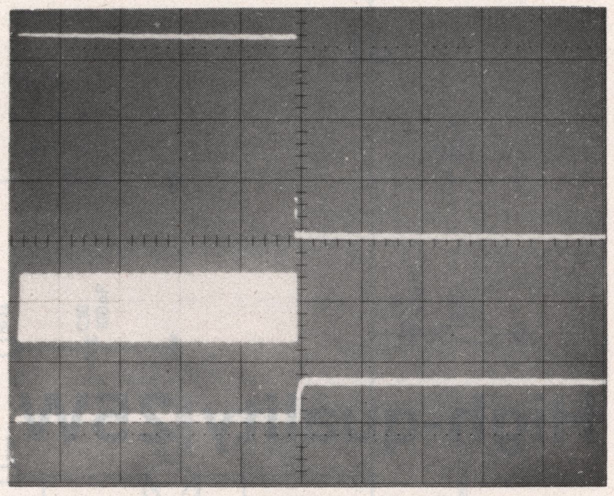

Fig.27 – Typical short-circuit waveforms

Upper trace: h.t. output voltage (50V/main division)
Lower trace: output transistor I_C (1A/main division)
Timebase: 50ms/main division

APPENDIX 1

Output Transformer for SMPS with Mains Isolation

Transformer characteristics

Primary inductance

At maximum primary current, L_P = 4·5mH ± 10%.

Leakage inductances

Inductance (approximate) of primary winding with other windings short-circuited:

S_2 shorted, L_P = 65μH;
S_1 shorted, L_P = 100μH;
S_3 shorted, L_P = 340μH.

Turns ratios

N_P/N_{S2} = 1·4;
N_{S2}/N_{S3} = 6·4;
N_{S2}/N_{S1} = 5·0.

Maximum winding currents

R.M.S. current in windings, measured for maximum load and minimum a.c. input:

$I_{P(max)}$ = 1·1A;
$I_{S2(max)}$ = 1·5A;
$I_{S3(max)}$ = 1·35A.

Power rating

Maximum total power output: 180W.

Winding resistances

Typical d.c. winding resistances:

R_P = 0·52Ω;
R_{S2} = 0·36Ω.

Isolation requirement

Isolation between mains and output circuits is to the requirements of BS 415.

The transformer is shown schematically in Fig.28. Note that the feedback secondary S_1 is on the primary side of the electrostatic screens.

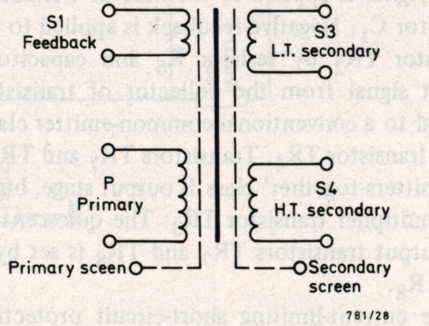

Fig.28 – Arrangement of output transformer (isolated)

High-quality 25W audio amplifier

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UDC 621.375.029.45

A high-quality 25W amplifier using BD266A and BD267A Darlington power transistors is described. The article includes details of the performance of the 25W amplifier, and an analysis of amplifier stability from Nichols charts.

INTRODUCTION

The high-quality audio amplifier described in this article has the following features: the output stage uses Darlington power transistors (BD266A and BD267A); the amplifier is powered by a split-output 26V-0-26V supply; the output devices are protected against short-circuit output by current-limiting transistors, and further protection is provided by fuses; bias to the output transistors is controlled by a V_{be} multiplier transistor; the input stage is a long-tail pair.

CIRCUIT DESCRIPTION

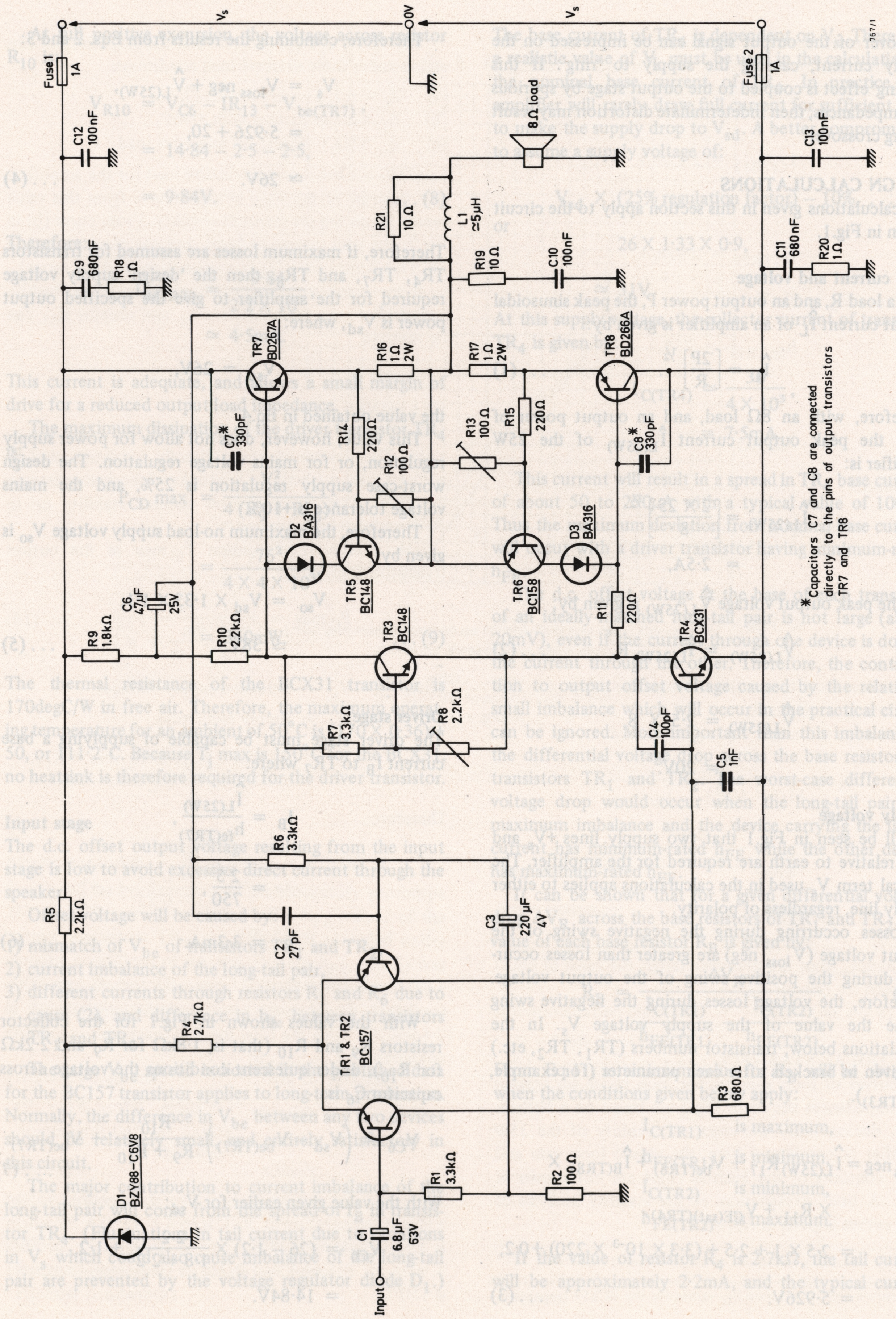
The circuit of the 25W amplifier is shown in Fig.1. Transistors TR_1 and TR_2 form the long-tail pair input stage. The long-tail pair configuration is necessary to give a low d.c. offset voltage across the output load. The input signal is applied to the base of transistor TR_1 by capacitor C_1. Negative feedback is applied to the base of transistor TR_2 by resistor R_6 and capacitor C_2. The output signal from the collector of transistor TR_1 is applied to a conventional common-emitter class A driver stage, transistor TR_4. Transistors TR_7 and TR_8 comprise an 'emitters-together' class B output stage, biased by the V_{be} multiplier transistor TR_3. The quiescent current of the output transistors TR_7 and TR_8 is set by potentiometer R_8.

The current-limiting short-circuit protection of the output transistors is provided by transistors TR_5 and TR_6. The output current is monitored by reference to the voltage across the emitter resistors R_{16} and R_{17}. Before the output current can exceed the limit value, transistors TR_5 and TR_6 conduct, preventing any further increase in the base currents of the output transistors. Unwanted forward conduction of the collector-base junctions of transistors TR_5 and TR_6 is prevented by diodes D_2 and D_3. Control of the limiting current of the output transistors is given by potentiometers R_{12} and R_{13}.

Should a short-circuit occur at the amplifier output, resistor R_{11} limits the maximum collector current of transistor TR_4. Under short-circuit conditions in the absence of resistor R_{11}, the collector voltage of transistor TR_4 would be held at nearly half the supply voltage. Resistor R_{11} also reduces the collector current of transistor TR_6.

The loop gain is controlled for stability purposes by capacitors C_2, C_4, C_5, C_7, and C_8. Stability is maintained for highly-capacitive loads by inductor L_1 and resistor R_{21}, and for highly-inductive loads by resistor R_{19} and capacitor C_{10}.

Supply decoupling components (capacitors C_9, C_{11}, C_{12}, C_{13}, and resistors R_{18} and R_{20}) may be omitted if close connection is made between the amplifier and the power supply reservoir capacitors. Low-impedance paths at high frequencies are provided by capacitors C_{12} and C_{13}. Although it is not essential to include capacitors C_9 and C_{11} and resistors R_{18} and R_{20} in the circuit, these components improve the h.f. performance of the amplifier by damping the tuned circuits formed by the supply inductances, and capacitors C_{12} and C_{13}. Without capacitors C_9 and C_{11} and resistors R_{18} and R_{20}, transient signals from the class B output stage during the


Fuse1 1A
V_s
0V
V_s
Fuse2 1A
C12 100nF
8Ω load
C13 100nF
R21 10Ω
L1 ≈5µH
C9 680nF
R18 1Ω
R19 10Ω
C10 100nF
C11 680nF
R20 1Ω
TR7 BD267A
R16 1Ω 2W
R17 1Ω 2W
TR8 BD266A
R14 220Ω
C7* 330pF
R12 100Ω
R13 100Ω
R15 220Ω
C8* 330pF
D2 BA316
TR5 BC148
TR6 BC158
D3 BA316
C6 47µF 25V
R9 1.8kΩ
R10 2.2kΩ
TR3 BC148
R11 220Ω
TR4 BCX31
R8 2.2kΩ
R7 3.3kΩ
C4 100pF
C5 1nF
R6 3.3kΩ
R5 2.2kΩ
C2 27pF
C3 220µF 4V
R4 2.7kΩ
TR1 & TR2 BC157
R3 680Ω
D1 BZY88-C6V8
R1 33kΩ
R2 100Ω
C1 6.8µF 63V
Input

* Capacitors C7 and C8 are connected directly to the pins of output transistors TR7 and TR8

Fig.1 – High-quality 25W amplifier

crossover of the output signal can be impressed on the supply current, causing the supply to 'ring'. If this 'ringing' effect is coupled to the output stage by spurious h.f. impedances, then indeterminate distortion may result during crossover.

DESIGN CALCULATIONS

The calculations given in this section apply to the circuit shown in Fig.1.

Load current and voltage

With a load R, and an output power P, the peak sinusoidal output current $\hat{I}_L$ of an amplifier is given by:

$$\hat{I}_L = \left[\frac{2P}{R}\right]^{\frac{1}{2}}. \qquad \ldots(1)$$

Therefore, with an 8Ω load, and an output power of 25W, the peak output current $\hat{I}_{L(25W)}$ of the 25W amplifier is:

$$\hat{I}_{L(25W)} = \left[\frac{2 \times 25}{8}\right]^{\frac{1}{2}},$$

$$= 2\cdot5\text{A},$$

and the peak output voltage $\hat{V}_{L(25W)}$ is given by:

$$\hat{V}_{L(25W)} = \hat{I}_{L(25W)}\,R, \qquad \ldots(2)$$

or

$$\hat{V}_{L(25W)} = 2\cdot5 \times 8,$$

$$= 20\text{V}.$$

Supply voltage

It will be seen in Fig.1 that two supply lines $+V_s$ and $-V_s$ relative to earth are required for the amplifier. The general term V_s used in the calculations applies to either supply line, regardless of polarity.

Losses occurring during the negative swing of the output voltage (V_{loss} neg) are greater than losses occurring during the positive swing of the output voltage. Therefore, the voltage losses during the negative swing define the value of the supply voltage V_s. In the calculations below, transistor numbers (TR_1, TR_2, etc.) are given in brackets after each parameter (for example, $V_{be(TR3)}$).

$$V_{loss}\,\text{neg} = \hat{I}_{L(25W)}R_{17} + V_{be(TR8)} + \hat{I}_{B(TR8)} \times$$

$$\times R_{11} + V_{CE(sat)(TR4)},$$

$$= 2\cdot5 \times 1 + 2\cdot5 + (3\cdot3 \times 10^{-3} \times 220) + 0\cdot2,$$

$$= 5\cdot926\text{V}. \qquad \ldots(3)$$

Therefore, combining the results from Eqs. 2 and 3:

$$V_s = V_{loss}\,\text{neg} + \hat{V}_{L(25W)},$$

$$= 5\cdot926 + 20,$$

$$\simeq 26\text{V}. \qquad \ldots(4)$$

Therefore, if maximum losses are assumed for transistors TR_4, TR_7, and TR_8, then the 'design' supply voltage required for the amplifier to give the specified output power is V_{sd}, where:

$$V_{sd} = 26\text{V},$$

the value obtained in Eq.4.

This value, however, does not allow for power supply regulation, or for mains voltage regulation. The design worst-case supply regulation is 25%, and the mains voltage tolerance is +10%.

Therefore, the maximum no-load supply voltage V_{so} is given by:

$$V_{so} = V_{sd} \times 1\cdot33 \times 1\cdot1,$$

$$\simeq 38\text{V}. \qquad \ldots(5)$$

Driver stage

The driver stage must be capable of supplying a base current I_B to TR_7 where:

$$I_B = \frac{\hat{I}_{L(25W)}}{h_{fe(TR7)}},$$

$$= \frac{2\cdot5}{750},$$

$$= 3\cdot3\text{mA}. \qquad \ldots(6)$$

With the values shown in Fig.1 for the collector resistors R_9 and R_{10} (that is, 1·8kΩ for R_9 and 2·2kΩ for R_{10}), under quiescent conditions the voltage across capacitor C_6 is:

$$V_{C6} = \left(V_{sd} - V_{be(TR7)}\right)\frac{R_{10}}{R_9 + R_{10}} + V_{be(TR7)}. \qquad \ldots(7)$$

With the value given earlier for V_{sd}:

$$V_{C6} = (26 - 1\cdot2) \times \frac{2\cdot2}{1\cdot8 + 2\cdot2} + 1\cdot2,$$

$$= 14\cdot84\text{V}.$$

At full positive excursion, the voltage across resistor R_{10} is:

$$V_{R10} = V_{C6} - \hat{I}R_{13} - V_{be(TR7)},$$

$$= 14\cdot84 - 2\cdot5 - 2\cdot5,$$

$$= 9\cdot84\text{V}. \qquad \ldots(8)$$

Therefore:

$$I_{B(TR7)} = \frac{9\cdot84}{2\cdot2 \times 10^3},$$

$$\simeq 4\cdot5\text{mA}.$$

This current is adequate, and allows a small margin of drive for a reduced output load impedance.

The maximum dissipation of the driver transistor TR_4 is:

$$P_{CD}\,\max = \frac{V_{so}^2}{4(R_9 + R_{10})},$$

$$= \frac{76^2}{4 \times 4 \times 10^3},$$

$$= 360\text{mW}. \qquad \ldots(9)$$

The thermal resistance of the BCX31 transistor is 170degC/W in free air. Therefore, the maximum operating temperature for an ambient of 50°C is (170 × 0·36) + 50, or 111·2°C. Because T_j max is 150°C for the BCX31, no heatsink is therefore required for the driver transistor.

Input stage

The d.c. offset output voltage resulting from the input stage is low to avoid excessive direct current through the speaker.

Offset voltage will be caused by:

1) mismatch of V_{be} of transistors TR_1 and TR_2,
2) current imbalance of the long-tail pair,
3) different currents through resistors R_1 and R_6 due to cause (2), and difference in h_{fe} between transistors TR_1 and TR_2.

The large V_{be} spread indicated in the published data for the BC157 transistor applies to long-term production. Normally, the difference in V_{be} between any two devices should be relatively small, and entirely satisfactory in this circuit.

The major contribution to current imbalance of the long-tail pair will come from the spread of I_B in transistor TR_4. (Fluctuations in tail current due to variations in V_s which could also cause imbalance of the long-tail pair are prevented by the voltage regulator diode D_1.)

The base current of TR_4 is dependent on V_s. Therefore, a realistic value of V_s must be used in the calculation of the nominal base current of TR_4. In practice, the amplifier will rarely draw full current for sufficient time to make the supply drop to V_{sd}. A better compromise is to assume a supply voltage of:

$$V_{sd} \times (25\%\ \text{regulation factor}) - 10\%, \qquad \ldots(10)$$

or

$$26 \times 1\cdot33 \times 0\cdot9,$$

$$\simeq 31\text{V}.$$

At this supply voltage, the collector current of transistor TR_4 is given by:

$$I_{C(TR4)} \simeq \frac{30}{4 \times 10^3},$$

$$= 7\cdot5\text{mA}.$$

This current will result in a spread in TR_4 base current of about 50 to 250μA with a typical value of 100μA. Thus the maximum deviation from nominal base current will occur with a driver transistor having minimum-rated h_{FE}.

The d.c. offset voltage at the base of each transistor of an ideally-matched long-tail pair is not large (about 20mV), even if the current through one device is double the current through the other. Therefore, the contribution to output offset voltage caused by the relatively small imbalance which will occur in the practical circuit can be ignored. More important than this imbalance is the differential voltage drop across the base resistors of transistors TR_1 and TR_2. The worst-case differential voltage drop would occur when the long-tail pair has maximum imbalance and the device carrying the larger current has minimum-rated h_{FE} while the other device has maximum-rated h_{FE}.

It can be shown that for a given differential voltage drop ΔV_R across the base resistors of TR_1 and TR_2, the value of each base resistor R_B is given by:

$$R_B = \frac{\Delta V_R}{\dfrac{I_{C(TR1)}}{h_{FE(TR1)}} - \dfrac{I_{C(TR2)}}{h_{FE(TR2)}}}. \qquad \ldots(11)$$

From Eq.11, a minimum value for R_B will be obtained when the conditions given below apply:

$I_{C(TR1)}$ is maximum,
$h_{FE(TR1)}$ is minimum,
$I_{C(TR2)}$ is minimum,
$h_{FE(TR2)}$ is maximum.

If the value of resistor R_4 is 2·7kΩ, the tail current will be approximately 2·2mA, and the typical current through each device will be 1·1mA. The maximum imbalance will occur with a driver transistor having a minimum-rated h_{FE} as mentioned previously. For a maximum imbalance of transistors TR_1 and TR_2:

$$I_{C(TR1)} = 1{\cdot}25\text{mA}.$$

Therefore:

$$I_{C(TR2)} = 0{\cdot}95\text{mA}.$$

When ΔV_R is 40mV max:

$$h_{fe(TR1)} = 75^*,$$

and

$$h_{fe(TR2)} = 260\dagger.$$

Therefore:

$$R_B \leqslant \frac{40 \times 10^{-3}}{\dfrac{1{\cdot}25 \times 10^{-3}}{75} - \dfrac{0{\cdot}95 \times 10^{-3}}{260}},$$

$$\leqslant 3{\cdot}08 \times 10^3\,\Omega. \qquad \ldots(12)$$

In practice, from the preferred range, the value of 3·3kΩ is chosen for resistors R_1 and R_6.

The value of resistor R_3 is given below:

$$R_3 = \frac{V_{be(TR4)}}{(1{\cdot}1 \times 10^{-3}) - I_{B(TR4)}},$$

$$= \frac{0{\cdot}6}{(1{\cdot}1 \times 10^{-3}) - (0{\cdot}1 \times 10^{-3})},$$

$$= 600\Omega. \qquad \ldots(13)$$

In practice, from the preferred range, the value of 680Ω is chosen for resistor R_3.

ELECTRICAL STABILITY

The curves of loop gain against loop phase for various load impedances shown in Fig.2 are based on a Nichols chart. Because only the electrical stability of the 25W amplifier is considered here, the closed loop gain and phase contours of the Nichols chart are not shown in Fig.2. A brief explanation of the stability analysis of these curves is given in Appendix 1.

The curves in Fig.2 indicate that the amplifier remains stable under three extreme load conditions:

(a) $Z_L = 8\Omega$, a purely-resistive load,
(b) $Z_L = 8\Omega$ in parallel with 4·7nF,
(c) $Z_L = 8\Omega + 200\mu H$, an inductive load.

Load (b) is a worst-case capacitive load for the amplifier: any increase or decrease in capacitance from this value results in an improvement in stability. From curve (b) in Fig.2, the gain margin is 14dB, and the phase margin is 78° (see Appendix 1 for an explanation of these terms).

If the amplifier is not required to work into highly-capacitive loads, then inductor L_1 and resistor R_{21} can be omitted.

HEATSINKS

Only the output transistors TR_7 and TR_8 require heatsinks. The devices must be directly mounted (that is, without mica washers) on heatsinks of thermal resistance 4degC/W. This figure ensures thermal stability up to 50°C ambient temperature.

The maximum dissipation P_C max in the output transistors is given by:

$$P_C \max = \frac{V_{so}^2}{\pi R\left(\dfrac{4m}{1-m} + \pi\right)}, \qquad \ldots(14)$$

where: V_{so} = unloaded supply voltage,
m = supply regulation,
R = R_L min + R_{16}, or R_L min + R_{17}, and R_L min = R_L nom − 20%.

Therefore:

$$P_C \max = \frac{76^2}{4\pi \times 7{\cdot}4\left(\dfrac{4 \times 0{\cdot}25}{1 - 0{\cdot}25} + \pi\right)},$$

$$= 13{\cdot}9\text{W}.$$

The effective thermal resistance of the BD266A (or BD267A) mounting base to aluminium heatsink is 2·4degC/W. Thus the total thermal resistance to ambient temperature $R_{th(j\text{-}amb)}$ is:

$$R_{th(j\text{-}amb)} = 4 + 2{\cdot}4,$$

$$= 6{\cdot}4\text{degC/W}.$$

Therefore, the maximum operating temperature for an ambient temperature of 50°C is (6·4 × 13·9) + 50, which is approximately 139°C. This is satisfactory because T_j max for BD266A and BD267A Darlington transistors is 150°C.

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*Minimum and † maximum h_{fe} values for the BC157 transistor.

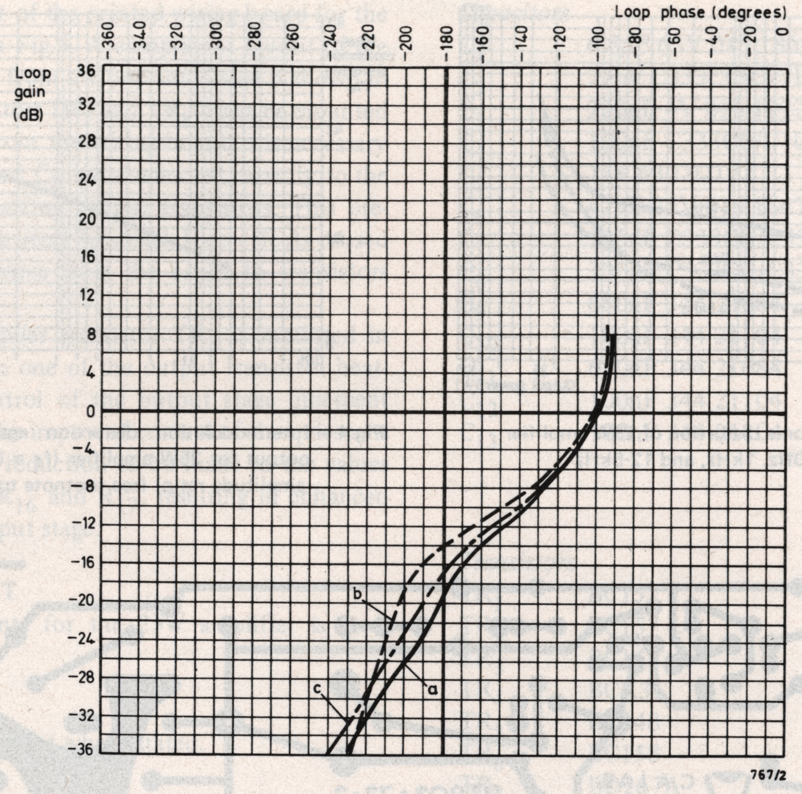

Fig.2 — Loop gain against loop phase for the 25W amplifier. Curves are shown for three output impedances:

(a) $Z_L = 8\Omega$,
(b) $Z_L = 8\Omega$ in parallel with 4·7nF,
(c) $Z_L = 8\Omega + 200\mu H$

PERFORMANCE

Details of the performance of the laboratory prototype 25W amplifier are given below. The h_{FE} values of the output transistors TR_7 and TR_8 were recorded under working conditions of 3A and 3V. The h_{FE} of TR_7 was 1500, and that of TR_8 was 1200. Acceptable matching of the output transistors was obtained with these h_{FE} values.

Frequency response: (P_o = 1W at the −3dB points with 0dB ref. 1kHz)	7Hz to 180kHz
Sensitivity: (P_o = 25W at 1kHz)	430mV
Noise: (output noise over 0 to 20kHz effective bandwidth)	1kΩ source: $\leqslant$0·1mV ∞ Ω source: 1·6mV
Feedback at 1kHz:	44dB
Input resistance:	≃ 350kΩ
Total harmonic distortion:	<0·12% up to 25W and 12·5kHz (see Fig.3)
Intermodulation distortion: (f_1 = 50Hz, f_2 = 7kHz; 4:1 amplitude ratio for up to 25W equivalent power*)	$\leqslant$0·3% (see Fig.4)

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*The equivalent power is equal to the power produced by a sine-wave having the same peak amplitude as the composite test waveform.

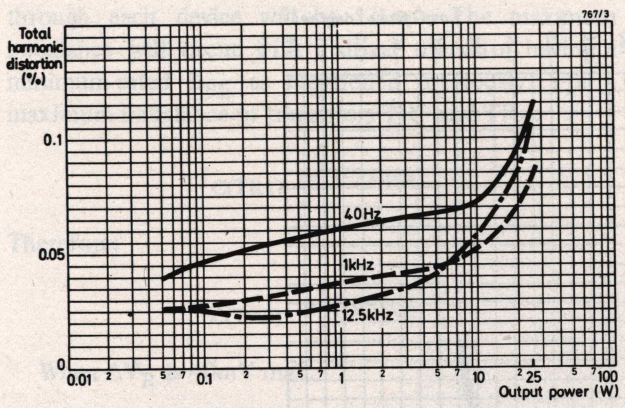

Fig.3 – Total harmonic distortion of 25W amplifier at 40Hz, 1kHz, and 12·5kHz

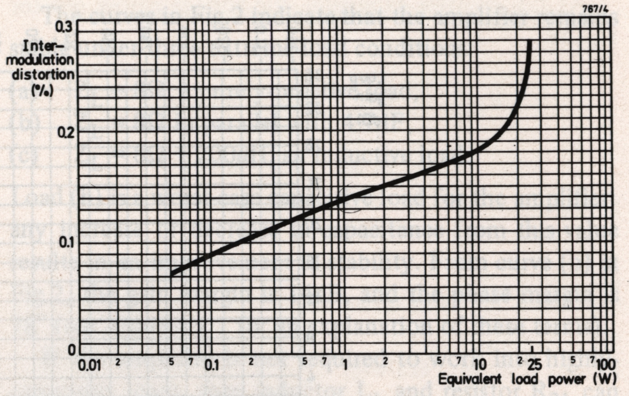

Fig.4 – Intermodulation distortion against equivalent power output for 25W amplifier (f_1 = 50Hz, f_2 = 7kHz, at 4:1 amplitude ratio) (see footnote to 'Performance' section)

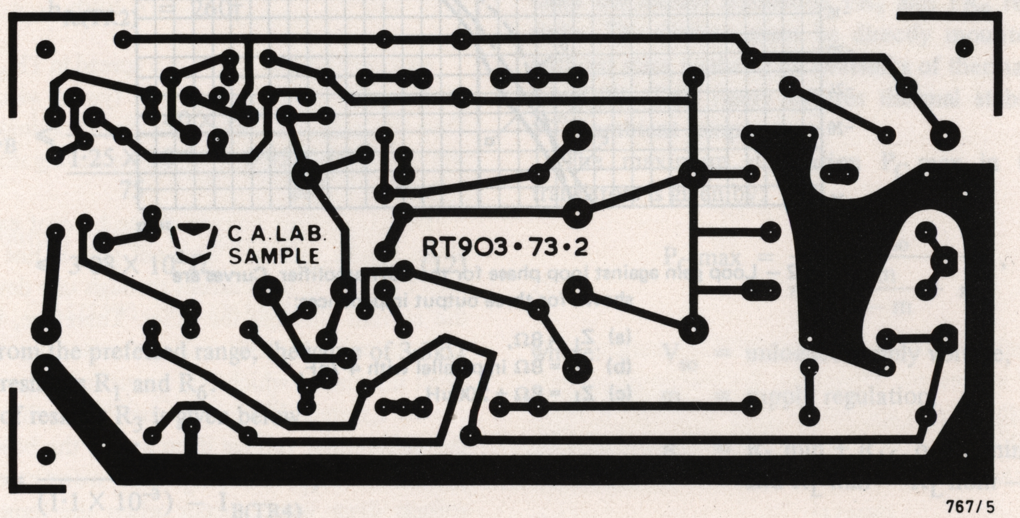

Fig.5 – Printing-wiring board for 25W amplifier

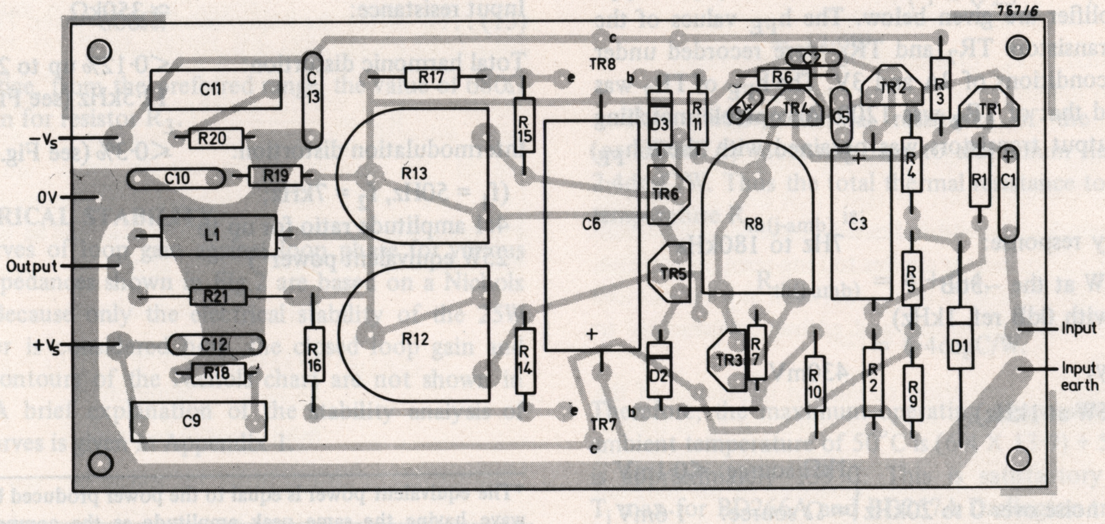

Fig.6 – View of printed-wiring board shown in Fig.5 from unprinted side, showing component positions

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A practical layout of the printed-wiring board for the amplifier is shown in Fig.5. A component layout of the printed-wiring board from the unprinted side is shown in Fig.6. Because transistors TR_7 and TR_8 must be mounted on heatsinks away from the wiring board, it is necessary that capacitors C_7 and C_8 are connected directly to the pins of the corresponding output transistors. This precaution will minimise stray feedback loop effects caused by the connecting wires from the board to transistors TR_7 and TR_8.

If the V_{be} multiplier transistor TR_3 is mounted in thermal contact with one of the output transistor heatsinks, improved control of the output stage quiescent current is possible. The improved control of the quiescent current will allow a reduction to be made in the values of emitter resistors R_{16} and R_{17}, resulting in enhanced efficiency of the output stage.

COMPONENTS LIST

A list of components for the 25W amplifier is given below.

Resistors

All resistors CR25 except where stated.

R_1	3·3kΩ	
R_2	100Ω	
R_3	680Ω	
R_4	2·7kΩ	
R_5	2·2kΩ	
R_6	3·3kΩ	
R_7	3·3kΩ	
R_8	2·2kΩ	carbon preset potentiometer (Egen Electric Ltd.) 2322 411 08305
R_9	1·8kΩ	
R_{10}	2·2kΩ	
R_{11}	220Ω	
R_{12}	100Ω	carbon preset potentiometer (Egen Electric Ltd.) 2322 411 08301
R_{13}		
R_{14}	220Ω	
R_{15}	220Ω	
R_{16}	1Ω, 2W	
R_{17}	1Ω, 2W	
R_{18}	1Ω	
R_{19}	10Ω	
R_{20}	1Ω	
R_{21}	10Ω	

Capacitors

C_1	6·8μF 63V 015 18688
C_2	27pF C333CC/C27E
C_3	220μF 4V 016 12221
C_4	100pF C333CC/C100E
C_5	1nF 630 02102
C_6	47μF 25V 016 16479
C_7	330pF C333CH/C330E
C_8	330pF C333CH/C330E
C_9	680nF 344 21684
C_{10}	100nF 344 21104
C_{11}	680nF 344 21684
C_{12}	100nF 344 21104
C_{13}	100nF 344 21104

Transistors

TR_1	BC157
TR_2	BC157
TR_3	BC148
TR_4	BCX31
TR_5	BC148
TR_6	BC158
TR_7	BD267A
TR_8	BD266A

Diodes

D_1	BZY88-C6V8
D_2	BA316
D_3	BA316

Inductor

L_1	5μH approx.	23 turns of 0.560mm diameter (24swg) enamelled copper wire wound on Neosid core type CH1/1/500 (16mm × 5mm diameter)

Fuses

Fuse 1	1A
Fuse 2	1A

Appendix 1 overleaf

APPENDIX 1

Analysis of Amplifier Stability from Nichols Charts

This Appendix describes briefly the cause of instability in a simple feedback system, and how amplifier stability can be assessed by using a Nichols chart.

The Nichols chart is intended to give information on the closed-loop performance of a feedback system (see Fig.7) from the loop gain characteristics. The closed-loop gain in Fig.7 is given by:

$$A_{CL} = \frac{A}{1 + A\beta} \quad \ldots (15)$$

For stability analysis, the term $A\beta$ is of interest. If the value of $A\beta$ becomes −1, then the closed loop gain becomes infinite; that is, the system becomes unstable.

On the Nichols chart, the logarithmic magnitude (in decibels) is plotted against the phase (in degrees) of $A\beta$, with varying frequency. From the curve obtained, the 'stability margin' can be readily seen. The 'critical point' on the chart is the 0dB, −180° point, equivalent to the −1, 0 point of the Nyquist chart. It is at this point that the phase has shifted 180° from the negative feedback value; that is, the feedback has become positive and the loop gain is unity. If the system is to be stable, the locus of the loop gain and phase must pass below the critical point to ensure a gain of less than unity for 180° phase shift. The further the locus passes below the critical point, the greater the stability margin becomes.

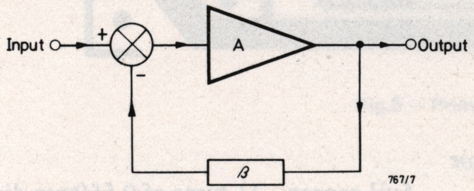

Fig.7 — Feedback system

A measure of the degree of stability is given by the gain margin and phase margin of the system as indicated in the simplified Nichol's chart in Fig.8 (see also Fig.2). The margins represent the amounts by which the gain and the phase shift could be increased to bring the system to the verge of instability. As shown in Fig.8, the margins can be obtained easily from the chart. The gain margin is read off at the intersection of the loop gain locus (curve a) with the −180° line, and the phase margin is read off at the intersection of the locus with the 0dB line. The reference point for each margin is the critical point.

The second locus (curve b) in Fig.8 is above the critical point, indicating an unstable system.

In Fig.2, the curves indicate a satisfactory stability margin for the 25W amplifier under various load conditions.

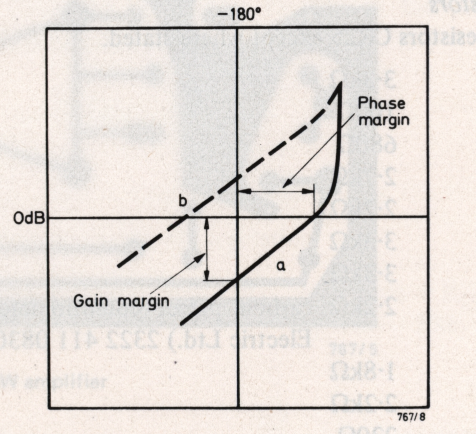

Fig.8 — Simplified Nichols chart, showing gain margin and phase margin for stable system (curve a). Curve b indicates unstable system

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An opto-isolated oscilloscope trigger circuit

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A simple opto-isolated oscilloscope trigger circuit for use with inverter and phase control power circuits is described.

INTRODUCTION

The circuits described here were originally developed to provide reliable trigger signals for an oscilloscope used to observe voltage waveforms in inverter and phase control power circuits. Normally in such circuits the most suitable source of trigger signals is the inverter drive stage. However, as the drive stage is usually isolated from the power stage, it is necessary in turn to isolate the drive stage from the oscilloscope. In the circuits described here therefore, a simple battery-driven photocoupler (opto-isolator) circuit is employed to isolate the trigger source.

CIRCUIT DESCRIPTION

Fig.1 shows the circuit at the output side of the isolating photocoupler. This is common to all applications and would normally be connected directly to the trigger input of the oscilloscope. It can also be used, however, to provide a reference signal on one of the beams. The input LED of the CNY43 photocoupler is driven from a suitable input circuit, the form of which depends on the particular inverter drive circuit. Various input circuits are described later.

The circuit in Fig.1 consumes negligible power until the input to the photocoupler is driven. Thus the battery will not be drained if the switch is inadvertently left closed for reasonable periods. The output signal is a positive-going pulse of up to 7V; the amplitude can be adjusted by means of R_3 to suit the particular oscilloscope. The CNY43 input LED requires a drive current of 6mA. Diode D_1 is an indicator lamp.

Three typical input circuits are shown in Figs.2, 3, and 4. The circuit of Fig.2 is used where the inverter drive circuit is built round TTL. It requires the signal source to sink about 400μA which is normally a negligible load. A positive-going trigger pulse appears at the oscillo-

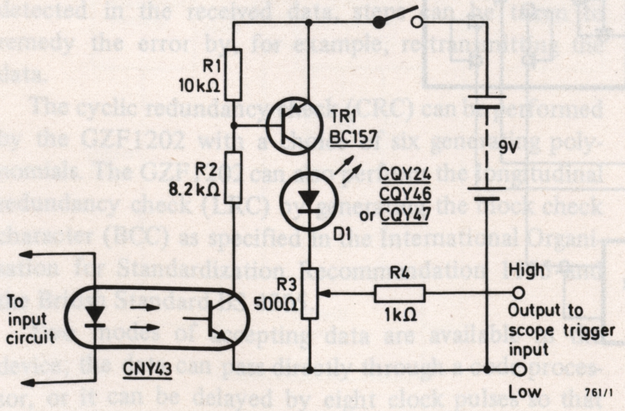

Fig.1 — Output circuit

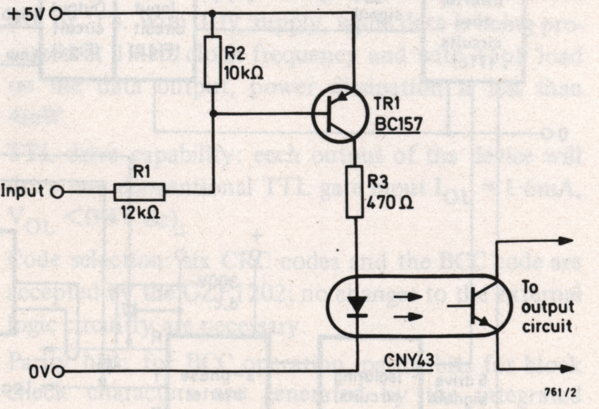

Fig.2 — Input circuit for use with TTL drive

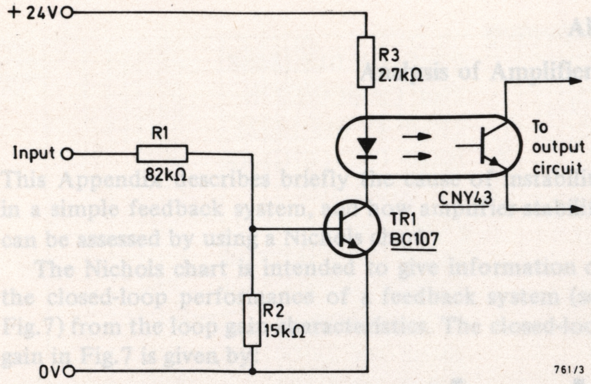

Fig.3 — Input circuit for use with Norbit 2 drive

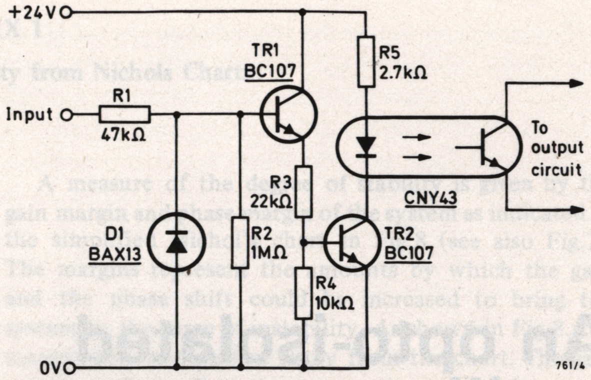

Fig.4 — High input resistance circuit for use with Norbit 2 or 61-series drive

scope input when the output from the inverter drive stage goes low.

The flexibility of the circuit in Fig.2 can be increased if required by the use of a low-power TTL gate at the input.

Figs.3 and 4 are intended for use with Norbit 2 and 61-series inverter drive systems. The circuit in Fig.3 has a standard one-drive-unit input, whereas that in Fig.4 has an input resistance of greater than 330kΩ which offers a negligible load to all Norbit 2 and most 61-series circuits. The supply required by both circuits is 24V ± 25%. A positive-going trigger pulse appears at the oscilloscope input when the output from the drive stage goes high.

If the resistor R_5 in Fig.4 is reduced to 1·5kΩ, the circuit is suitable for use with 15V logic circuits.

APPLICATION EXAMPLE

A typical measurement arrangement is shown in Fig.5. A suitable trigger signal is generated by the drive circuit once per cycle of the three-phase fundamental output frequency. This is passed via the opto-isolator circuit to channel 1 of the oscilloscope, and subsequently to the trigger control circuit. A stable trace is produced, as shown in Fig.6. With the timebase set sufficiently slow, a second trigger pulse will occur on channel 1 which will allow the period of the waveform to be measured. Note that channel 3 is a differential input which automatically displays the line-to-line voltage waveform (R-Y).

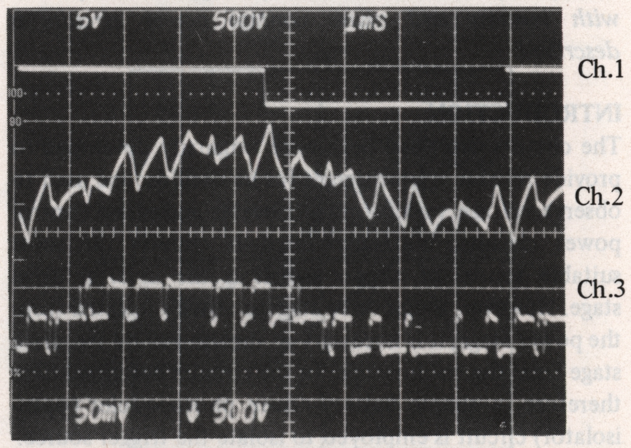

Fig.6 — Typical oscillogram showing the waveforms on oscilloscope channels 1, 2, and 3 in the circuit shown in Fig.5

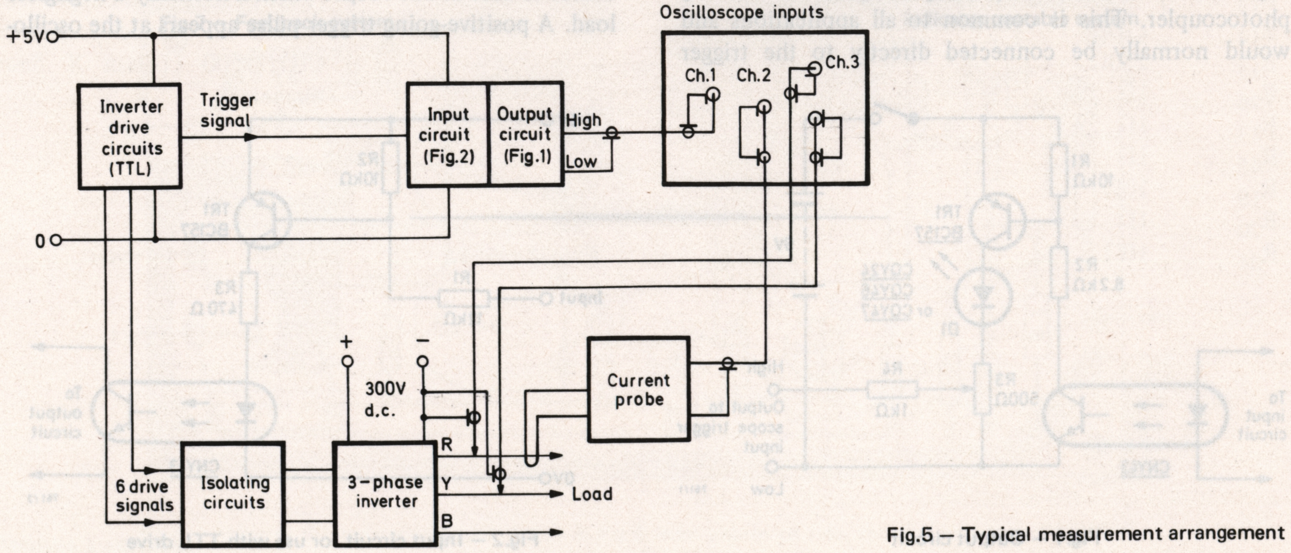

Fig.5 — Typical measurement arrangement

Product Information:

GZF1202 encoder and decoder for data error detection

A recent Mullard publication (Ref.1) which is available on request describes an error-detecting integrated circuit for use in data transmission systems. This brief synopsis of the device GZF1202 is abstracted from the full publication.

Data communications systems are subject to the introduction of errors by transient voltage interference from a variety of external sources (for example, lightning, switching, and crosstalk from other communication lines).

The GZF1202 integrated circuit is an encoder and decoder for error checking in serial data transmission systems. Two GZF1202 devices are used in a data transmission system, one at each end of the line. The devices are effectively in the data path. The error detection bits are transmitted after each data message. Similarly, the error detection bits are examined when the data is received. In this way, the data remains unaltered, and is compatible with receivers (such as data terminals) that have no error detection facilities. When an error has been detected in the received data, steps can be taken to remedy the error by, for example, re-transmitting the data.

The cyclic redundancy check (CRC) can be performed by the GZF1202 with a choice of six generating polynomials. The GZF1202 can also perform the longitudinal redundancy check (LRC) by generating the block check character (BCC) as specified in the International Organisation for Standardization Recommendation 1155 and the British Standard BS 4505.

Two modes of accepting data are available in the device; the data can pass directly through a code processor, or it can be delayed by eight clock pulses so that synchronising characters, start of text (STX) characters, and end of text (ETX) characters can be detected and inhibited from the code processor. These characters are termed 'unwanted' characters in this description.

All inputs and outputs of the integrated circuit are protected against electrostatic voltages.

The GZF1202 is a LOCMOS (Local Oxidation Complementary Metal Oxide Silicon) device, contained in a dual-in-line 18-lead encapsulation. The device is available now in production quantities.

PRINCIPAL FEATURES OF GZF1202

The GZF1202 has a number of outstanding features, and these are listed below.

- High-speed operation: at 5V supply, data transmission speed through the device is about 1·6Mbits/s. At 10V supply, data transmission speed is approximately doubled. Selected devices capable of operating at higher speeds will be available on request.
- Low power consumption: power dissipation is less than 10μW at all supply voltages, with all inputs static ('0' or '1'). With 10V supply, while data is being processed at 1MHz clock frequency and with 15pF load on the data output, power dissipation is less than 4mW.
- TTL drive capability: each output of the device will drive one conventional TTL gate input I_{OL} = 1·6mA, V_{OL} <0·4V dc).
- Code selection: six CRC codes and the BCC code are accepted by the GZF1202; no changes to the external logic circuitry are necessary.
- Parity bits: for BCC operation, parity bits for block check characters are generated by the integrated circuit.

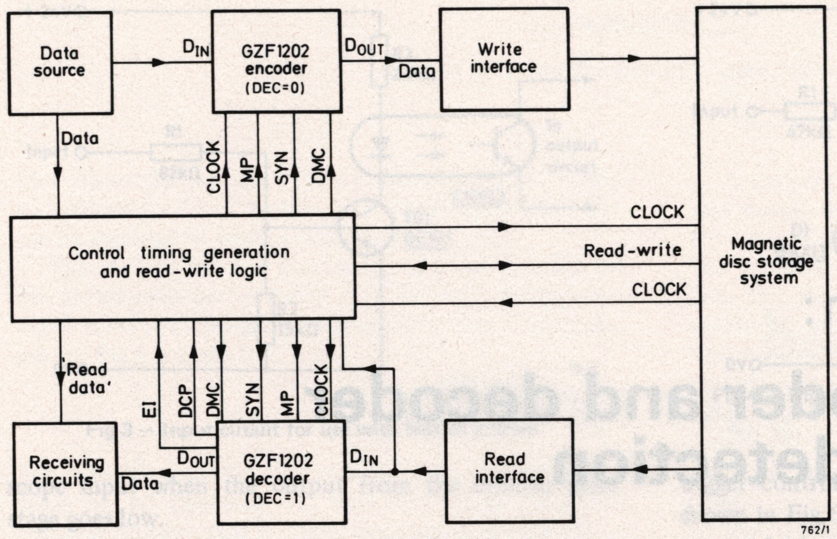
Data source
D_{IN}
GZF1202 encoder (DEC=0)
D_{OUT}
Data
Write interface
Data
CLOCK
MP
SYN
DMC
CLOCK
Read-write
CLOCK
Control timing generation and read-write logic
Magnetic disc storage system
'Read data'
EI
DCP
DMC
SYN
MP
CLOCK
Receiving circuits
D_{OUT}
Data
GZF1202 decoder (DEC=1)
D_{IN}
Read interface
762/1

Fig.1 — Magnetic disc serial data storage system using two GZF1202 devices

- Data unaltered: in the encoding process only 'check bits' are added to the data and these are easily segregated from the data during decoding. The data is preserved in its original state throughout the encoding and decoding processes. The polarity of the data is the same at the input and output of the device.
- Inhibit function: when the 'unwanted' character reject (SYN) pin 3 is LOW, data passes directly to the output of the device without being processed.

GZF1202 APPLICATIONS

Two applications of the GZF1202 integrated circuit are given below. Further application information for the device is given in Ref.1.

Magnetic disc serial data storage system

Fig.1 shows the GZF1202 used as an encoder and decoder in a magnetic disc serial data storage system. Two devices are shown in the diagram, but a single GZF1202 can be switched to perform encoding and decoding functions. The system works at high speed (above 2Mbits/s) and so the device is operated at 10V supply. The input shift register is used to remove data skew and to allow unwanted characters to be inhibited if necessary.

Teletype-computer data link

A second application of the GZF1202 integrated circuit is the teletype-computer data link shown in Fig.2. In this low-speed (typically 300bits/s) application, a teletype system and a buffer store are used to send a 'packet' of data down a line to a computer peripheral. The encoder and decoder are operated at 5V supply, and the input shift register is used in each device.

REFERENCE

1. 'GZF1202 Encoder and Decoder for Data Error Detection', Technical Information 5, TP1479, Mullard Limited, 1975.

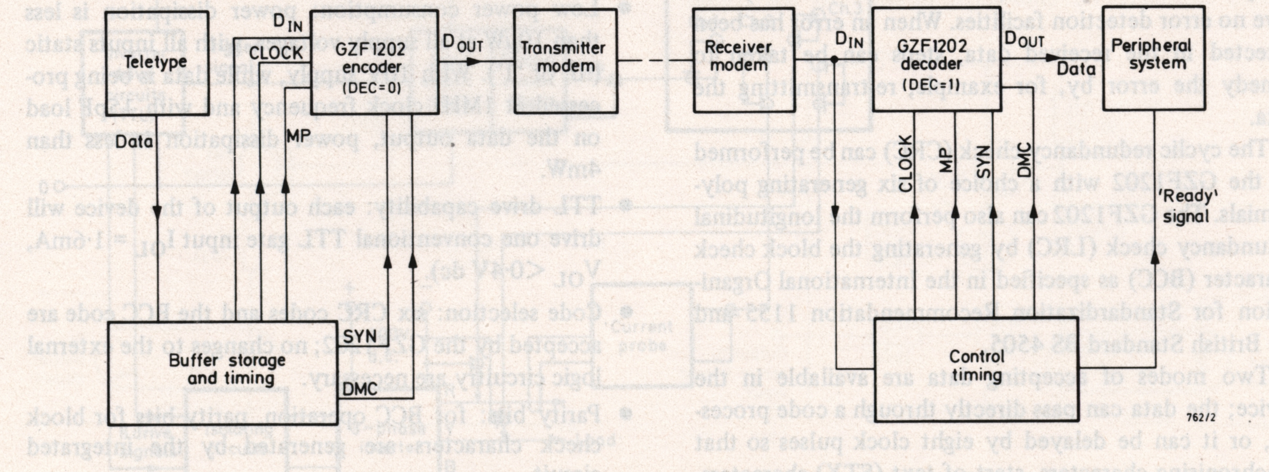
Teletype
CLOCK
D_{IN}
GZF1202 encoder (DEC=0)
D_{OUT}
Transmitter modem
Data
MP
SYN
Buffer storage and timing
DMC
Receiver modem
D_{IN}
GZF1202 decoder (DEC=1)
D_{OUT}
Data
Peripheral system
CLOCK
MP
SYN
DMC
'Ready' signal
Control timing
762/2

Fig.2 — Two GZF1202 devices used in a teletype-computer data link